**BVVS**

# Basaveshwar Engineering College, Bagalkote

# Department of Electronics and Communication Engineering

## Vision, Mission Statements and Values

## Vision

To achieve excellence in electronics and communication engineering through quality education and research for developing competent professionals.

## Mission

1. Foster a dynamic teaching and learning process.
2. Encourage research through innovation and collaboration.
3. Imbibe moral, ethical values and social responsibilities.

## Values

The values of the department are

1. Work is Worship
2. Ethics and Integrity
3. Empathy and Compassion
4. Indian Ethos
5. Mutual Respect

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# Basaveshwar Engineering College, Bagalkote

## Department of Electronics and Communication Engineering

## SWOC Analysis

## S:Strength:

1. Infrastructure
   - (i.) ICT enabled classrooms/seminar hall with good ambience.
   - (ii.) Well equipped laboratories to cater curriculum requirements.
   - (iii.) Department library with good number of titles and volumes.
   - (iv.) Scope for academic extension programmes.
2. Faculty
   - (i.) 75% of faculty with Ph.D.
   - (ii.) Faculty with minimum of 12 years teaching experience.
   - (iii.) Faculty retention ratio is 100 %.
3. Students
   - (i.) Students with academic and competitive bent of mind.
   - (ii.) 75% of the students are placed in reputed industries.
   - (iii.) 10% to 15% of the students are registering for B.E. Honours Degree.
4. Curriculum
   - (i.) Research and industry oriented adaptive curriculum.
   - (ii.) Curriculum with integrated courses.
5. Alumni
   - (i.) Alumni works in reputed organizations across the world.
   - (ii.) Alumni interactions with students and faculty to bridge the gap between campus and corporate.

## W:Weakness:

1. IPR competencies are inadequate.
2. Relatively less number of memberships in professional bodies.
3. Limited collaborative activities.
4. Less number of inter-disciplinary courses and projects.
5. Less number of industry supported laboratories/courses.
6. Inadequate number of funded projects.
7. Less scope for co-curricular and cultural activities.

## O:Opportunities:

1. Establishment of Distant Learning Center (DLC) using existing resources.
2. Participation in collaborative projects/ research work with allied institutions.
3. Fostering alumni participation in academics and placement activities.
4. Establishment of Skilling Centers for students.
5. Faculty exchange programs with academia and industry.
6. Organizing conferences.
7. Facilitating incubation centers for alumni.
8. Scope for academic extension programmes
9. Training on computer usage/ programming languages for general public.
10. Enhancing consultancy activities.

## C:Challenges:

1. To incorporate experiential teaching learning process.
2. Adapting curriculum to future industry needs.
3. Fostering collaboration to enhance research, innovation and entrepreneurship activities.
4. Attracting diversified students.
5. Strategies to strengthen the placement activities for higher packages and core companies.
6. Secure additional research grants and consultancy opportunities.
7. Enhance quality publications and file patents.

## Programme Outcomes

a) **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

b) **Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

c) **Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

d) **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

e) **Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

f) **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

g) **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

h) **Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

i) **Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

j) **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

k) **Project management and finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

l) **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

## Programme Specific Outcomes (PSOs)

1. Analyze and design systems for electronics, communication, and signal processing applications.
2. Use domain specific tools for design, analysis, synthesis, and validation of VLSI and embeddedsystems
3. Demonstrate the conceptual knowledge with respect to architecture, design analysis and simulationof computer networking and applications

## Programme Educational Objectives (PEOs)

**PEO1:** Our graduates will be able to lead a successful career by solving complex Engineering Problems of society/industry

**PEO2:** Enable graduates to excel in academia, industry, entrepreneurship and engage in research and lifelong learning

**PEO3:** Graduates will be able to work effectively as individuals in multidisciplinary environments with high integrity, ethics, human values and societal responsibilities

**PEO4:** Graduates will be able to exhibit strong leadership, communication, and teamwork skills to succeed in dynamic professional environments and contribute to the global challenges

# Basaveshwar Engineering College, Bagalkote
## B.E. in Electronics and Communication Engineering
## Scheme of Teaching and Examinations
## AY: 2023-24

**III SEMESTER**

| Sl. No | Course | Course Code | Course Title | Teaching Department (TD)and Question Paper Setting Board (PSB) | Teaching Hours /Week | | | | Examination | | | | Credits |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Theory Lecture | Tutorial | Practical/ Drawing | SDA | Duration inhours | CIE Marks | SEE Marks | Total Marks | |
| | | | | | L | T | P | S | | | | | |
| 1 | PCC | 22UMA312C | AV Mathematics-III for EC Engineering | MATHEMATICS | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 2 | IPCC | 22UEC311C | Digital System Design using Verilog | ECE DEPT. | 3 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 4 |
| 3 | IPCC | 22UEC312C | Electronic Principles and Circuits | ECE DEPT. | 3 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 4 |
| 4 | PCC | 22UEC313C | Network Analysis | ECE DEPT. | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 5 | PCCL | 22UEC314L | Analog and Digital Systems Design Lab | ECE DEPT. | 0 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 1 |
| 6 | ESC | 22UEC315X | ESC/ETC/PLC | ECE DEPT. | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 7 | UHV | 22UHS317L | Social Connect and Responsibility | HSS DEPT. | 0 | 0 | 2 | 0 | 01 | 100 | --- | 100 | 1 |
| 8 | AEC/ SEC | 22UEC316X | Ability Enhancement Course/Skill EnhancementCourse– III | ECE DEPT. | If the course is a Theory: 1 | 0 | 0 | 0 | 01 | 50 | 50 | 100 | 1 |
| | | | | | If a course is a laboratory: 0 | 0 | 2 | 0 | 02 | | | | |
| 9 | MC | 22UHS001M | Yoga | YOGA TEACHER | 0 | 0 | 2 | 0 | | 25 | --- | 25 | 0 |
| | | 22UHS002M | National Service Scheme (NSS) | NSS COORDINATOR | | | | | | | | | |
| | | 22UHS003M | Physical Education (PE) (Sports and Athletics) | PHYSICAL EDUCATION DIRECTOR | | | | | | | | | |
| | | 22UHS004M | Music | MUSIC TEACHER | | | | | | | | | |
| | | | | **Total** | **15/16** | **0** | **12** | | **22** | **475** | **350** | **825** | **20** |

| Sl. No. | Ability Enhancement Course (AEC) | Subject Code | Engineering Science Course (ESC) | Subject Code | Skill Enhancement Course (SEC) | Subject Code |
|---|---|---|---|---|---|---|
| 1. | C++ Basics | 22UEC316A | Electronic Devices | 22UEC315A | MATLAB Programming | 22UEC316C |
| 2. | IOT for Smart Infrastructure | 22UEC316B | Computer Organization and Architecture | 22UEC315B | LABVIEW programming | 22UEC316D |
| 3. | | | Sensors and Instrumentation | 22UEC315C | | |
| 4. | | | Applied Numerical Methods for EC Engineers | 22UEC315D | | |

**PCC**: Professional Core Course, **PCCL**: Professional Core Course laboratory, **UHV**: Universal Human Value Course, **MC**: Mandatory Course(Non-credit),**AEC**: Ability Enhancement Course, **SEC**: Skill Enhancement Course,**L:**Lecture,**T**:Tutorial,**P**:Practical**S=SDA**:SkillDevelopmentActivity,**CIE**:ContinuousInternalEvaluation,**SXX**:

# Basaveshwar Engineering College, Bagalkote
## B.E. in Electronics and Communication Engineering
## Scheme of Teaching and Examinations
## AY: 2023-24

**IV SEMESTER**

| Sl. No | Course and Course Code | | Course Title | Teaching Department (TD) and Question Paper Setting Board (PSB) | Teaching Hours /Week | | | | Examination | | | | Credits |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Theory Lecture | Tutorial | Practical/ Drawing | Self -Study | Duration in hours | CIE Marks | SEE Marks | Total Marks | |
| | | | | | L | T | P | S | | | | | |
| 1 | PCC | 22UEC410C | Electromagnetic Theory | ECE DEPT. | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 2 | IPCC | 22UEC411C | Principles of Communication Systems | ECE DEPT. | 3 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 4 |
| 3 | IPCC | 22UEC412C | Control Systems | ECE DEPT. | 3 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 4 |
| 4 | PCCL | 22UEC413C | Communication Lab | ECE DEPT. | 0 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 1 |
| 5 | ESC | 22UEC4XXC | ESC/ETC/PLC | ECE DEPT. | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 6 | AEC/ SEC | 22UEC4XXC | Ability Enhancement Course/Skill Enhancement Course- IV | ECE DEPT. | If the course is Theory | | | | 01 | 50 | 50 | 100 | 1 |
| | | | | | 1 | 0 | 0 | 0 | | | | | |
| | | | | | If the course is a lab | | | | 02 | | | | |
| | | | | | 0 | 0 | 2 | 0 | | | | | |
| 7 | BSC | 22UBT407C | Biology For Engineers | ECE DEPT. | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 8 | UHV | 22UHS424C | Universal human values course | ECE DEPT. | 1 | 0 | 0 | 0 | 01 | 50 | 50 | 100 | 1 |
| 9 | MC | 22UHS001M | Yoga | YOGA TEACHER | | | | | | | | | |
| | | 22UHS002M | National Service Scheme (NSS) | NSS COORDINATOR | | | | | | | | | |
| | | 22UHS003M | Physical Education (PE) (Sports and Athletics) | PHYSICAL EDUCATION DIRECTOR | 0 | 0 | 2 | 0 | | 25 | --- | 25 | 0 |
| | | 22UHS004M | Music | MUSIC TEACHER | | | | | | | | | |
| | | | | **Total** | **16/17** | **0** | **10** | | **24** | **500** | **400** | **900** | **20** |

**PCC**: Professional Core Course, **PCCL**: Professional Core Course laboratory, **UHV**: Universal Human Value Course, **MC**: Mandatory Course(Non-credit),**AEC**: Ability Enhancement Course, **SEC**: Skill Enhancement Course,**L:**Lecture,**T**:Tutorial,**P**:Practical**S=SDA**:SkillDevelopmentActivity,**CIE**:ContinuousInternalEvaluation,**SXX**:

| Sl. No. | Ability Enhancement Course AEC | Subject Code | Engineering Science Course ESC | Subject Code | Skill Enhancement Course (SEC) | Subject Code |
|---|---|---|---|---|---|---|
| 1. | Octave Programming | 22UEC415A | Data Structures using C | 22UEC414A | Data Structures Lab using C | 22UEC415C |
| 2. | Programmable Logic Controllers | 22UEC415B | Microcontrollers | 22UEC414B | Microcontroller Lab | 22UEC415D |
| 3. | | | Industrial Electronics | 22UEC414C | | |
| 4. | | | Operating Systems | 22UEC414D | | |
| 5. | | | Signals and Systems | 22UEC414E | | |

**Basaveshwar Engineering College, Bagalkote**
**B.E. in Electronics and Communication Engineering**
**Scheme of Teaching and Examinations**
**AY: 2023-24**

| V SEMESTER | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Sl. No | Course and Course Code | | Course Title | Teaching Department(TD) and Question Paper Setting Board(PSB) | Teaching Hours/Week | | | | Examination | | | | Credits |
| | | | | | Theory Lecture | Tutorial | Practical/Drawing | SDA | Duration in hours | CIE Marks | SEE Marks | Total Marks | |
| | | | | | L | T | P | S | | | | | |
| 1 | HSMS | 22UEC512C | Technological Innovation and Management Entrepreneurship | ECE DEPT. | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 2 | IPCC | 22UEC513C | Digital Signal Processing | ECE DEPT. | 3 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 4 |
| 3 | PCC | 22UEC514C | Digital Communication | ECE DEPT. | 4 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 4 |
| 4 | PCCL | 22UEC515L | Digital Communication Lab | ECE DEPT. | 0 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 1 |
| 5 | PEC | 22UEC5XXE | Professional Elective Course | ECE DEPT. | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 6 | PROJ | 22UEC517P | Mini Project | ECE DEPT. | 0 | 0 | 4 | 0 | 03 | 100 | -- | 100 | 2 |
| 7 | AEC | 22UHS507C | **Research Methodology and IPR** | ECE DEPT. | 2 | 2 | 0 | 0 | 02 | 50 | 50 | 100 | 3 |
| 8 | MC | 22UBT508C | Environmental Studies | ANY DEPARTMENT | 2 | 0 | 0 | 0 | 02 | 50 | 50 | 100 | 2 |
| 9 | MC | 22UHS001M | Yoga | YOGA TEACHER | 0 | 0 | 2 | 0 | | 25 | --- | 25 | 0 |
| | | 22UHS002M | National Service Scheme (NSS) | NSS COORDINATOR | | | | | | | | | |
| | | 22UHS003M | Physical Education (PE) (Sports and Athletics) | PHYSICAL EDUCATION DIRECTOR | | | | | | | | | |
| | | 22UHS004M | Music | MUSIC TEACHER | | | | | | | | | |
| 10 | AC | 22UHS521C | Qualitative Aptitude and Soft Skills | TPC | 2 | 0 | 0 | 0 | 2 | 100 | -- | 100 | 0 |
| **Total** | | | | | **19** | **2** | **10** | **0** | **24** | **650** | **350** | **1000** | **22** |

| Professional Elective Course | | |
|---|---|---|
| 1. | Intelligent Systems and Machine Learning Algorithms | 22UEC521E |
| 2. | Digital Switching and Finite Automata Theory | 22UEC522E |
| 3. | Data Structure using C++ | 22UEC523E |
| 4. | Satellite and Optical Communication | 22UEC524E |

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## AY: 2023-24

**VI SEMESTER**

| Sl.No | Course and Course Code | | Course Title | Teaching Department(TD) and Question Paper Setting Board(PSB) | Teaching Hours/Week | | | | Examination | | | | Credits |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Theory Lecture | Tutorial | Practical/Drawing | SDA | Duration in hours | CIE Marks | SEE Marks | Total Marks | |
| | | | | | L | T | P | S | | | | | |
| 1 | IPCC | 22UEC611C | Embedded System Design | ECE DEPT | 3 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 4 |
| 2 | PCC | 22UEC612C | VLSI Design and Testing | ECE DEPT | 4 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 4 |
| 3 | PEC | 22UEC6XXE | Professional Elective Course | ECE DEPT | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 4 | OEC | 22UECXXXN | Open Elective Course | RESPECTIVE DEPT | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 5 | PROJ | 22UEC619P | Major Project Phase I | ECE DEPT | 0 | 0 | 4 | 0 | 03 | 100 | -- | 100 | 2 |
| 6 | PCCL | 22UEC620L | VLSI Design and Testing Lab | ECE DEPT | 0 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 1 |
| 7 | AEC | 22UHS600C | Indian Knowledge System | ECE DEPT | If the course is offered as a Theory | | | | 01 | 50 | 50 | 100 | 1 |
| | | | | | 1 | 0 | 0 | 0 | | | | | |
| | | | | | If course is offered as a practical | | | | | | | | |
| | | | | | 0 | 0 | 2 | 0 | | | | | |
| 8 | MC | 22UHS001M | Yoga | YOGA TEACHER | 0 | 0 | 2 | 0 | | 25 | --- | 25 | 0 |
| | | 22UHS002M | National Service Scheme (NSS) | NSS COORDINATOR | | | | | | | | | |
| | | 22UHS003M | Physical Education (PE) (Sports and Athletics) | PHYSICAL EDUCATION DIRECTOR | | | | | | | | | |
| | | 22UHS004M | Music | MUSIC TEACHER | | | | | | | | | |
| **Total** | | | | | **14/13** | **0** | **12/10** | **0** | **19** | **500** | **300** | **800** | **18** |

| Sl. No. | **Professional Elective Course (PEC)** | Subject Code | **Open Elective Course (OE)** | Subject Code |
|---|---|---|---|---|
| 1. | Multimedia Communication | 22UEC621E | Digital System Design using Verilog | 22UECXXXN |
| 2. | Digital Image Processing | 22UEC622E | Electronic Communication Systems | 22UECXXXN |
| 3. | Computer and Data Security | 22UEC623E | Consumer Electronics | 22UECXXXN |
| 4. | FPGA System Design using Verilog | 22UEC624E | Basic VLSI Design | 22UECXXXN |

**Basaveshwar Engineering College, Bagalkote**
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**AY: 2023-24**

**VII SEMESTER (Swappable VII and VIII SEMESTER)**

| Sl. No | Course and Course Code | | Course Title | Teaching Department(TD) and Question Paper Setting Board(PSB) | Teaching Hours/Week | | | | Examination | | | | Credits |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Theory Lecture | Tutorial | Practical/Drawing | SDA | Duration in hours | CIE Marks | SEE Marks | Total Marks | |
| | | | | | L | T | P | S | | | | | |
| 1 | IPCC | 22UEC720C | Microwave Engineering and Antenna Theory | ECE DEPT | 3 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 4 |
| 2 | IPCC | 22UEC721C | Computer Networks and Protocols | ECE DEPT | 3 | 0 | 2 | 0 | 03 | 50 | 50 | 100 | 4 |
| 3 | PCC | 22UEC722C | Wireless Communication Systems | ECE DEPT | 4 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 4 |
| 4 | PEC | 22UEC7XXE | **Professional Elective Course** | RESPECTIVE DEPT | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 5 | OEC | 22UECXXXN | **Open Elective Course** | ECE DEPT | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 6 | PROJ | 22UEC724P | **Major Project Phase-II** | ECE DEPT | 0 | 0 | 12 | 0 | 03 | 100 | 100 | 200 | 6 |
| | | | | | 16 | 0 | 16 | 0 | 18 | **350** | **350** | **700** | **24** |

| Sl. No. | Professional Elective Course (PEC) | Subject Code | Open Elective Course (OE) | Subject Code |
|---|---|---|---|---|
| 1. | Application Specific Integrated Circuit | 22UEC731E | E-waste Management | 22UECXXXN |
| 2. | Automotive Electronics | 22UEC732E | Embedded System Applications | 22UECXXXN |
| 3. | Cyber Security | 22UEC733E | Automotive Electronics | 22UECXXXN |
| 4. | Radar Communication | 22UEC734E | Sensors and Actuators | 22UECXXXN |

**L:**Lecture,**T**:Tutorial,**P**:Practical**S=SDA**:SkillDevelopmentActivity,**CIE**:ContinuousInternalEvaluation,**SEE**:SemesterEndEvaluation.**TD**-TeachingDepartment,**PSB**: PaperSettingdepartment,**OEC**:OpenElectiveCourse,**PEC**:ProfessionalElectiveCourse.**PROJ**:Projectwork,**INT**:IndustryInternship/ResearchInternship/RuralInternship

**Basaveshwar Engineering College, Bagalkote**
**B.E. in Electronics and Communication Engineering**
**Scheme of Teaching and Examinations**
**AY: 2023-24**

| VIII SEMESTER (Swappable VII and VIII SEMESTER) | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Sl.No | Course and Course Code | | Course Title | Teaching Department(TD) and Question Paper Setting Board(PSB) | Teaching Hours/Week | | | | Examination | | | | Credits |
| | | | | | Theory Lecture | Tutorial | Practical/Drawing | SDA | Duration in hours | CIE Marks | SEE Marks | Total Marks | |
| | | | | | L | T | P | S | | | | | |
| 1 | PEC | 22UECXXXX | **Professional Elective (Online Courses) MOOCS** | | 3 | 0 | 0 | 0 | 03 | 50 | 50 | 100 | 3 |
| 2 | OEC | 22UECXXXX | **Open Elective (Online Courses) MOOCS** | | 3 | 0 | 0 | 0 | 01 | 50 | 50 | 100 | 3 |
| 3 | INT | 22UEC811T | **Internship (Industry/Research) (14-20weeks)** | | 0 | 0 | 12 | 0 | 03 | 100 | 100 | 200 | 10 |
| | | | **Total** | | 6 | 0 | 12 | 0 | 07 | **200** | **200** | **400** | **16** |
| **Professional Elective Course** | | | | | | | | | | | | | |
| | | BOS Recommended Course | | | | BOS Recommended Course | | | | | | | |
| | | BOS Recommended Course | | | | BOS Recommended Course | | | | | | | |
| **Open Elective Courses** | | | | | | | | | | | | | |
| | | BOS Recommended Course | | | | BOS Recommended Course | | | | | | | |
| | | BOS Recommended Course | | | | BOS Recommended Course | | | | | | | |

**L:**Lecture,**T**:Tutorial,**P**:Practical**S=SDA**:SkillDevelopmentActivity,**CIE**:ContinuousInternalEvaluation,**SEE**:SemesterEndEvaluation.**TD-**TeachingDepartment,**PSB**:
PaperSettingdepartment,**OEC**:OpenElectiveCourse,**PEC**:ProfessionalElectiveCourse.**PROJ**:Projectwork,**INT**:IndustryInternship/ResearchInternship/RuralInternship

# III Semester Syllabus

| AV Mathematics-III for EC Engineering | | Semester | 3 |
|---|---|---|---|
| Course Code | **22UMA312C** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

1. Learn to use the Fourier series to represent periodical physical phenomena in engineering analysis and to enable the student to express non-periodic functions to periodic functions using the Fourier series and Fourier transforms.
2. Analyze signals in terms of Fourier transforms
3. Develop the knowledge of solving differential equations and their applications in Electronics & Communication engineering.
4. To find the association between attributes and the correlation between two variables

**Teaching-Learning Process Pedagogy**
**(General Instructions):**

These are sample Strategies; teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills.
2. State the need for Mathematics with Engineering Studies and Provide real-life examples.
3. Support and guide the students for self–study.
4. You will assign homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students to group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   i. As an introduction to new topics (pre-lecture activity).
   ii. As a revision of topics (post-lecture activity).
   iii. As additional examples (post-lecture activity).
   iv. As an additional material of challenging topics (pre-and post-lecture activity).
   v. As a model solution of some exercises (post-lecture activity).

**Module-1: Fourier series and practical harmonic analysis**

Periodic functions, Dirichlet's condition. Fourier series expansion of functions with period $2\pi$ and with arbitrary period: periodic rectangular wave, Half-wave rectifier, rectangular pulse, Saw tooth wave. Half-range Fourier series. Triangle and half range expansions, Practical harmonic analysis, variation of periodic current. **(8 hours)**

**Module-2: Infinite Fourier Transforms**

Infinite Fourier transforms, Fourier cosine and sine transforms, Inverse Fourier transforms, Inverse Fourier cosine and sine transforms, discrete Fourier transform (DFT), Fast Fourier transform (FFT).

**(8 hours)**

**Module-3: Z Transforms**

Definition, Z-transforms of basic sequences and standard functions. Properties: Linearity, scaling, first and second shifting, multiplication by n. Initial and final value theorem. Inverse Z- transforms. Application to difference equations. **(8 hours)**

**Module-4:**

Ordinary Differential Equations of Higher Order

Higher-order linear ODEs with constant coefficients - Inverse differential operator, problems. Linear differential equations with variable Coefficients-Cauchy's and Legendre's differential equations–Problems. Application of linear differential equations to L-C circuit and L-C-R circuit. **(8 hours)**

**Module-5:**

**Curve fitting, Correlation, and Regressions**

Principles of least squares, Curve fitting by the method of least squares in the form $y = a + bx$, $y = a + bx + cx^2$, and $y = ax^b$. Correlation, Coefficient of correlation, Lines of regression, Angle between regressions lines, standard error of estimate, rank correlation. **(8 hours)**

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Demonstrate the Fourier series to study the behavior of periodic functions and their applications in system communications, digital signal processing, and field theory.
2. To use Fourier transforms to analyze problems involving continuous-time signals
3. To apply Z-Transform techniques to solve difference equations
4. Understand that physical systems can be described by differential equations and solve such equations
5. Make use of correlation and regression analysis to fit a suitable mathematical model for statistical data

**Internal Assessment Test question paper is designed to attain the different levels ofBloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module(with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books (Name of the author/Title of the Book/Name of the publisher/Edition and Year)Text Books:**

1. **B. S. Grewal**: "Higher Engineering Mathematics", Khanna Publishers, 44thEd., 2021.
2. **E. Kreyszig**: "Advanced Engineering Mathematics", John Wiley & Sons, 10thEd., 2018.

**Reference Books:**

1. **V. Ramana:** "Higher Engineering Mathematics" McGraw-Hill Education, 11th Ed., 2017
2. **Srimanta Pal & Subodh C.Bhunia**: "Engineering Mathematics" Oxford University Press, 3rd Ed., 2016.
3. **N.P Bali and Manish Goyal**: "A Textbook of Engineering Mathematics" Laxmi Publications, 10th Ed., 2022.
4. **C. Ray Wylie, Louis C. Barrett:** "Advanced Engineering Mathematics" McGraw–HillBook Co., New York, 6th Ed., 2017.
5. **Gupta C.B, Sing S.R and Mukesh Kumar:** "Engineering Mathematic for Semester I andII", McGraw Hill Education(India) Pvt. Ltd 2015.
6. **H.K. Dass and Er. Rajnish Verma:** "Higher Engineering Mathematics" S. Chand Publication, 3rd Ed.,2014.
7. **James Stewart: "**Calculus" Cengage Publications, 7th Ed., 2019.

**Web links and Video Lectures (e-Resources):**

- http://nptel.ac.in/courses.php?disciplineID=111
- http://www.class-central.com/subject/math(MOOCs)
- http://academicearth.org/
- VTU e-Shikshana Program
- VTU EDUSAT Program.

**Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning**

- Quizzes
- Assignments
- Seminar

| Digital System Design using Verilog | | Semester | 3 |
|---|---|---|---|
| Course Code | **22UEC311C** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory + 8-10 Lab slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |
| Examination nature (SEE) | Theory/Practical | | |

**Course objectives:**

This course will enable students to:

1. To impart the concepts of simplifying Boolean expression using K-map techniques and Quine- McCluskey minimization techniques.
2. To impart the concepts of designing and analyzing combinational logic circuits.
3. To impart design methods and analysis of sequential logic circuits.
4. To impart the concepts of Verilog HDL-data flow and behavioral models for the design of digital systems.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Linear Algebra & Signal Processing.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.
10. Give Programming Assignments.

**MODULE-1**

**Principles of Combinational Logic**: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. (Section 3.1 to 3.5 of Text1).

**MODULE-2**

| |
|---|
| **Logic Design with MSI Components and Programmable Logic Devices**: Binary Adders and Subtractors, Comparators, Decoders, Encoders, Multiplexers, Programmable Logic Devices (PLDs) (Section 5.1 to 5.7 of Text 2) |
| **MODULE-3** |
| **Flip-Flops and its Applications**: The Master-Slave Flip-flops (Pulse-Triggered flip-flops): SR flip- flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text 2), State diagrams. |
| **MODULE-4** |
| **Introduction to Verilog**: Structure of Verilog module, Operators, Data Types, Styles o Description. (Section 1.1 to1.6.2, 1.6.4 (only Verilog), 2 of Text 3)<br>**Verilog Data flow description:** Highlights of Data flow description, Structure of Data flow description. (Section 2.1 to 2.2 (only Verilog) of Text 3) |
| **MODULE-5** |
| **Verilog Behavioral description**: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioral Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3)<br>**Verilog Structural description**: Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder.(Section 4.1 to 4.2 of Text3 ) |

**PRACTICAL COMPONENT OF IPCC** *(Experiments can be conducted either using any circuit simulation software or discrete components)*

| Sl. No. | Experiments |
|---|---|
| 1 | To simplify the given Boolean expressions and realize using Verilog program |
| 2 | To realize Adder/Subtract or (Full/half) circuits using Verilog data flow description. |
| 3 | To realize 4-bit ALU using Verilog program. |
| 4 | To realize the following Code converters using Verilog Behavioral description<br>a) Gray to binary and vice versa b) Binary to excess3 and vice versa |
| 5 | To realize using Verilog Behavioral description: 8:1 mux, 8:3 encoder, and Priority encoder |
| 6 | To realize using Verilog Behavioral description: 1:8 De-mux, 3:8 decoder, 2–bit Comparator |
| 7 | To realize using Verilog Behavioral description:<br>Flip-flops: a) JK type b) SR type c) T type and d) D-type |
| 8 | To realize Counters-up/down (BCD and binary) using Verilog Behavioral description. |
| 9 | Write Verilog code for the given sequential circuit problem statement or state diagram. |
| **Demonstration Experiments (For CIE only–not to be included for SEE)**<br>Use FPGA/CPLD kits for down loading Verilog codes and check the output for inter facing experiments. | |
| 10 | Verilog Program to interface a Stepper motor to the FPGA/CPL D and rotate the motor in the specified direction (by N steps). |

| | |
|---|---|
| 11 | Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working. |

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

1) Simplify Boolean functions using K-map and the Quine-McCluskey minimization technique.
2) Analyze and design combinational logic circuits.
3) Analyze the concepts of flip-flops (SR, D, T, and JK) and design synchronous sequential circuits using flip-flops.
4) Model combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

**Assessment Details (Both CIE and SEE):**

The weightage of Continuous Internal Evaluation (CIE) is 50%, and the weightage for the Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 out of 50), and for the SEE, the minimum passing mark is 35% of the maximum marks (18 out of 50). A student is declared to have passed the course if he/she secures a minimum of 40% (40 marks out of 100) in the combined total of the CIE and SEE. The **IPCC** refers to the practical portion integrated with the theory of the course. CIE marks for the theory component are 25 marks, and the practical component is also 25 marks.

**CIE for the Theory Component of the IPCC:**

1. The 25 marks for the theory component are split into 15 marks for two Internal Assessment Tests (each test is 15 marks with duration of 1 hour) and 10 marks for other assessment methods mentioned in 22OB4.2. The first test is conducted after 40-50% of the syllabus is covered, and the second test after 85-90% of the syllabus is covered.
2. The scaled-down marks from the sum of the two tests and other assessment methods will be the CIE marks for the theory component of the IPCC (out of 25 marks).
3. The student must secure 40% of the 25 marks to qualify in the CIE for the theory component of the IPCC.

**CIE for the Practical Component of the IPCC:**

1. 15 marks are allocated for the conduction of experiments and the preparation of the laboratory record, and 10 marks are allocated for a test to be conducted after the completion of all laboratory sessions.
2. Upon completing each experiment/program in the laboratory, students will be evaluated, including a viva-voce, and marks will be awarded on the same day.
3. The CIE marks for the practical component will be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. The total marks for all experiment write-ups will be added and scaled down to 15 marks.
4. A laboratory test (duration of 2-3 hours) will be conducted after the completion of all experiments, with a maximum score of 50 marks, scaled down to 10 marks.
5. The scaled-down marks from the write-up evaluations and the test will be added to form the CIE marks for the laboratory component of the IPCC, out of 25 marks.
6. The student must secure 40% of the 25 marks to qualify in the CIE for the practical component of the IPCC.

**SEE for IPCC:**

The Theory SEE will be conducted by the university as per the scheduled timetable, with common question papers for the course (duration: 3 hours).

1. The question paper will have ten questions, each worth 20 marks.
2. There will be two questions from each module. Each of the two questions under a module (with a maximum of three sub-questions) will cover a mix of topics from that module.
3. Students must answer five full questions, selecting one full question from each module.
4. The marks scored by the student will be proportionally scaled down to 50 marks.

**The theory portion of the IPCC will be assessed through both CIE and SEE, while the practical portion will have a CIE component only. Questions in the SEE paper may include content from the practical component.**

1. The minimum marks required in CIE to be eligible for SEE are 10 (40% of the maximum marks—25) in the theory component and 10 (40% of the maximum marks—25) in the practical component. The laboratory component of the IPCC is assessed through CIE only, but SEE may include questions from the practical component. A maximum of 4-5 sub-questions from the practical component of the IPCC can be set, with a total weightage of no more than 20 marks.
2. SEE will be conducted for 100 marks, and students must secure 35% of the maximum marks to qualify for SEE. Marks scored in SEE will be scaled down to 50.
3. A student is declared to have passed the course if he/she secures a minimum of 40% (40 marks out of 100) in the combined total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination).

**Suggested Learning Resources:**

**Books:**


1. *Digital Logic Applications and Design* by John M. Yarbrough, Thomson Learning, 2001.
2. *Digital Principles and Design* by Donald D. Givone, McGraw Hill, 2002.
3. *HDL Programming: VHDL and Verilog* by Nazeih M. Botros, 2009 reprint, Dreamtech Press.


**Reference Books:**


1. *Fundamentals of Logic Design* by Charles H. Roth Jr., Cengage Learning.
2. *Logic Design* by Sudhakar Samuel, Pearson/Sanguine, 2007.
3. *Fundamentals of HDL* by Cyril P. R., Pearson/Sanguine, 2010.


**Web links and Video Lectures (e-Resources):**

**www.chipverify.com**

**Activity-Based Learning (Suggested Activities in Class) / Practical-Based Learning:**

Programming assignments and mini-projects can be assigned to improve programming skills.

**Course Articulation Matrix:**

| Course Outcomes | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **A** | **b** | **c** | **d** | **e** | **f** | **g** | **h** | **i** | **j** | **k** | **l** | **m** | **n** | **o** |
| **CO1:** Simplify Boolean functions using K-map and the Quine-McCluskey minimization technique. | **2** | **3** | **1** | **2** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **3** | **0** |
| **CO2:** Analyze and design combinational logic circuits. | **2** | **3** | **1** | **2** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **3** | **0** |
| **CO3:** Analyze the concepts of flip-flops (SR, D, T, and JK) and design synchronous sequential circuits using flip-flops. | **2** | **3** | **1** | **2** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **3** | **0** |
| **CO4:** Model combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions. | **2** | **2** | **1** | **2** | **3** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **3** | **0** |

| Electronic Principles and Circuits | | Semester | 3 |
|---|---|---|---|
| Course Code | **22UEC312C** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory + 8-10 Lab slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | |
| Examination nature (SEE) | Theory/Practical/Viva-Voce /Term-work/Others | | |

**Course objectives:**

This course will enable students to

1. Design and analyze the BJT circuits as an amplifier and voltage regulation.
2. Design of MOSFET Amplifiers and analyze the basic amplifier configurations using small signal equivalentcircuit models
3. Design of operational amplifiers circuits as Comparators, DAC and filters.
4. Understand the concept of positive and negative feedback.
5. Analyze Power amplifier circuits in different modes of operation.
6. Construct Feedback and Oscillator circuits using FET.
7. Understand the thyristor operation and the different types of thyristors.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies; which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such asthe ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**MODULE -1**

**Transistor Biasing:** Voltage Divider Bias, VDB Analysis, VDB Load line and Q point, Two supply Emitter Bias, Other types of Bias.

**BJT AC models**: Base Biased Amplifier, Emitter Biased Amplifier, Small Signal Operation, AC Beta, AC Resistance of the emitter diode, two transistor models, Analyzing an amplifier, H parameters, Relations between R and H parameters.

**Voltage Amplifiers**: Voltage gain, Loading effect of Input Impedance.

**CC Amplifiers:** CC Amplifier, Output Impedance.

[Text1]

**MODULE -2**

**MOSFET**

Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor. Small signal operation and modelling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, trans conductance, The T equivalent circuit model. MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance, The Common Gate Amplifier, Source follower. [Text 2]

**MODULE-3**

**Linear Op-amp Circuits:** Summing Amplifier and D/A Converter, Nonlinear Op-amp Circuits: Comparator with zero reference, Comparator with non-zero references. Comparator with Hysteresis.

**Oscillator:** Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator.

**The 555 timer**: Monostable Operation, Astable Operation. [Text1]

**MODULE-4**

**Negative Feedback:** Four Types of Negative Feedback, VCVS Voltage gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation).

**Active Filters:** Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low Pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Band Pass Filters, Band stop Filters. [Text1]

**MODULE-5**

**Power Amplifiers:** Amplifier terms, two load lines, Class A Operation, Class B operation, Class B push pull emitter follower, Class C Operation.

**Thyristors:** The four-layer Diode, SCR, SCR Phase control, Bidirectional Thyristors, IGBTs, Other Thyristors. [Text1]

**PRACTICAL COMPONENT OF IPCC** *(Experiments can be conducted either using any circuit simulationsoftware or discrete components)*

| Sl.NO | Experiments |
|---|---|
| 1 | Design and Test<br>Bridge Rectifier with Capacitor Input Filter<br>Zener voltage regulator |
| 2 | Design and Test<br>Biased Clippers – a)Positive, b) Negative , c) Positive-NegativePositive and Negative Clampers with and without Reference. |
| 3 | Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductanceand amplification factor. |
| 4 | Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor. |
| 5 | Design and test Emitter Follower |
| 6 | Design and plot the frequency response of Common Source JFET/MOSFET amplifier |
| 7 | Test the Op-amp Comparator with zero and non-zero reference and obtain the Hysteresis curve. |
| 8 | Design and test Full wave Controlled rectifier using RC triggering circuit. |
| 9 | Design and test Precision Half wave and full wave rectifiers using Op-amp |
| 10 | Design and test RC phase shift oscillator |

**Course outcomes (Course Skill Set):**

At the end of the course, the student will be able to:

1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits.
2. Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.
3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.
4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.
5. Understand the power electronic device components and its functions for basic power electronic circuits.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory componentare **25 marks** and that for the practical component is **25 marks**.

**CIE for the theory component of the IPCC**

25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

**CIE for the practical component of the IPCC**

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva- voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write- ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.

2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will**

**have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component**.

1. The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
2. SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
3. The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Suggested Learning Resources:**

**Books**


**1.** Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017, ISBN:978-0-07-063424-4.

Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1


**Web links and Video Lectures (e-Resources):**


1. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
2. Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.


**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

**Course Articulation Matrix:**

| Course Outcomes | POs | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| **CO1:** Determine currents and voltages using source transformation / mesh/nodal analysis and reduce given network using star delta transformation. | 3 | 2 | 1 | 2 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 3 | 0 | 0 |
| **CO2:** Solve problems by applying Network Theorems and electrical laws to reduce circuit complexities and to arrive at feasible solutions | 3 | 3 | 1 | 2 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 3 | 0 | 0 |
| **CO3:** Analyze the circuit parameters during switching transients | 3 | 3 | 1 | 2 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 3 | 0 | 0 |
| **CO4:** Apply Laplace transform to solve the given network | 3 | 2 | 1 | 2 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 3 | 0 | 0 |
| **CO5:** Evaluate the frequency response for resonant circuits and the network parameters for two port networks | 3 | 2 | 1 | 2 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | | | |
| **Course Contribution to POs** | 3.00 | 2.4 | 1 | 2 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 3 | 0 | 0 |
| | | | | | | | | | | | | | | | |

| Network Analysis | | Semester | 3 |
|---|---|---|---|
| Course Code | **22UEC313C** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Module-1**

**Basic Concepts:** Practical sources, Source transformations, Network reduction using Star - Delta transformation, Loop and node analysis with linearly dependent and independentsources for DC and AC networks.

**Module-2**

**Network Theorems:** Superposition, Millman's theorems, Thevenin's and Norton's theorems, Maximum Power transfer theorem.

**Module-3**

**Transient behavior and initial conditions:** Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.

**Module-4**

**Laplace Transformation &Applications:** Solution of networks, step, ramp and impulse responses, waveform Synthesis.

**Module-5**

**Two port network parameters:** Definition of Z, Y, h and Transmission parameters, modeling with these parameters, relationship between parameters sets.

**Resonance:**

**Series Resonance:** Variation of Current and Voltage with Frequency, Selectivity and Bandwidth, Q-Factor, Circuit Magnification Factor, Selectivity with Variable Capacitance, Selectivity with Variable Inductance.

**Parallel Resonance:** Selectivity and Bandwidth, Maximum Impedance Conditions with C, L and f Variable, current in Anti-Resonant Circuit, The General Case-Resistance Present in both Branches.

**Course outcomes**

At the end of the course, the student will be able to:

1. Determine currents and voltages using source transformation / mesh/nodal analysis and reduce given network using star delta transformation.
2. Solve problems by applying Network Theorems and electrical laws to reduce circuit and to arrive at feasible solutions.
3. Analyze the circuit parameters during switching transients
4. Apply Laplace transform to solve the given network
5. Evaluate the frequency response for resonant circuits and the network parameters for two port networks

**Suggested Learning Resources:Books**


1. M. E. Van Valkenburg (2000), Network Analysis, Prentice Hall of India, 3rd edition, 2000, ISBN:9780136110958.
2. Roy Choudhury-Networks and Systems, 2nd edition, New Age International Publications,2006,

ISBN: 9788122427677

**Reference Books:**


3. Hayt, Kemmerly and Durbin – "Engineering Circuit Analysis", **TMH** 7th Edition, 2010.
4. J. David Irwin/ R.Mark Nelms – "Basic Engineering Circuit Analysis", John Wiley, 8th Ed, 2006.
5. Charles K Alexander and Mathew, N. O. Sadiku- "Fundamentals of Electric Circuits", Tata
6. McGraw-Hill, 3rd Ed, 2009.


**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/courses/108105159
- https://nptel.ac.in/courses/108102042
- https://psim.software.informer.com/11.1/
- https://www.ni.com/multisim

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

1. Demonstrate the operation of the following circuits using suitable simulation software (Open source such as Psim, Pspice, Proteus, Simulink, eSim)

- Determination of current through each branch of a given network using mesh analysis
- Determination of current through each branch of a given network using nodal analysis
- Simplification of given network using source transformation and finding the current in load
- Verification of Superposition, Millman's, Thevenin's and, Maximum Power transfer theorems using practical based approach

**Course Articulation Matrix:**

| **Course Outcomes** | **POs** | | | | | | | | | | | | **PSOs** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **a** | **b** | **c** | **d** | **e** | **f** | **g** | **h** | **i** | **j** | **k** | **l** | **m** | **n** | **o** |
| **CO1:** Determine currents and voltages using source transformation / mesh/nodal analysis and reduce given network using star delta transformation. | **3** | **2** | **1** | **2** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **3** | **0** | **0** |
| **CO2:** Solve problems by applying Network Theorems and electrical laws to reduce circuit complexities and to arrive at feasible solutions | **3** | **3** | **1** | **2** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **3** | **0** | **0** |
| **CO3:** Analyze the circuit parameters during switching transients | **3** | **3** | **1** | **2** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **3** | **0** | **0** |
| **CO4:** Apply Laplace transform to solve the given network | **3** | **2** | **1** | **2** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **3** | **0** | **0** |
| **CO5:** Evaluate the frequency response for resonant circuits and the network parameters for two port networks | **3** | **2** | **1** | **2** | **1** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | | | |
| **Course Contribution to Pos** | **3.00** | **2.4** | **1** | **2** | **1** | **1** | **0** | **1** | **1** | **1** | **0** | **1** | **3** | **0** | **0** |

| **Analog and Digital Systems Design Laboratory** | | Semester | **3** |
|---|---|---|---|
| Course Code | **22UEC314L** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 0:0:2 | SEE Marks | 50 |
| Credits | 01 | Exam Hours | 100 |
| Examination type (SEE) | Practical/Viva-Voce | | |

**Course objectives:**

This laboratory course enables students to

1. Understand the electronic circuit schematic and its working
2. Realize and test amplifier and oscillator circuits for the given specifications
3. Realize the op-amp circuits for the applications such as DAC, implement mathematical functions and precision rectifiers.
4. Study the static characteristics of SCR and test the RC triggering circuit.
5. Design and test the combinational and sequential logic circuits for their functionalities.
6. Use the suitable ICs based on the specifications and functions.

| **Sl.NO** | **Experiments (***All the experiments has to be conducted using discrete components***)** |
|---|---|
| 1 | Design and set up the BJT common emitter voltage amplifier with and without feedback and determine the gain- bandwidth product, input and output impedances. |
| 2 | Design and set-up BJT/FET i) Colpitts Oscillator, ii) Crystal Oscillator |
| 3 | Design and set up the circuits using op-amp: i) Adder, ii) Integrator, iii) Differentiator and iv) Comparator |
| 4 | Design 4-bit R – 2R Op-Amp Digital to Analog Converter (i) for a 4-bit binary input using toggle switches<br>(ii) by generating digital inputs using mod-16 |
| 5 | Design and implement (a) Half Adder & Full Adder using basic gates and NAND gates, (b) Half subtractor &<br>Full subtractor using NAND gates, (c) 4-variable function using IC74151(8:1MUX). |
| 6 | Realize (i) Binary to Gray code conversion & vice-versa (IC74139), (ii) BCD to Excess-3 code conversion<br>and vice versa |
| 7 | a) Realize using NAND Gates: i) Master-Slave JK Flip-Flop, ii) D Flip-Flop and iii) T Flip-Flop b) Realize the shift registers using IC7474/7495: (i) SISO (ii) SIPO (iii) PISO (iv) PIPO (v) Ring counter and (vi) Johnson<br>counter. |
| 8 | Realize a) Design Mod – N Synchronous Up Counter & Down Counter using 7476 JK Flip-flop b) Mod-N<br>Counter using IC7490 / 7476 c) Synchronous counter using IC74192 |

| | Demonstration Experiments ( For CIE ) |
|---|---|
| 9 | Design and Test the second order Active Filters and plot the frequency response,<br>i) Low pass and High pass Filter<br>ii) Band pass and Band stop Filter |
| 10 | Design and test the following using 555 timer<br>i) Monostable Multivibraator<br>ii) Astable Multivibrator |
| 11 | Design and Test a Regulated Power supply |
| 12 | Design and test an audio amplifier by connecting a microphone input and observe the output using a loudspeaker. |

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

1. Design and analyze the BJT/FET amplifier and oscillator circuits.
2. Design and test Op-amp circuits to realize the mathematical computations, DAC and precision rectifiers.
3. Design and test the combinational logic circuits for the given specifications.
4. Test the sequential logic circuits for the given functionality.
5. Demonstrate the basic circuit experiments using 555 timer.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural

knowledge will carry a weightage of 60% and the rest 40% for viva-voce.

- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero. The minimum duration of SEE is 02 hours

**Suggested Learning Resources:**


1. David A Bell, "Fundamentals of Electronic Devices and Circuits Lab Manual", 5th Edition, 2009, Oxford University Press.
2. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017.
3. Fundamentals of Logic Design, Charles H Roth Jr., Larry L Kinney, Cengage Learning, 7th Edition.

| Electronic Devices | | Semester | 3 |
|---|---|---|---|
| Course Code | 22UEC315A | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:** This course will enable students to:

1. Understand the basics of semiconductor physics and electronic devices.
2. Describe the mathematical models BJTs and FETs along with the constructional details.
3. Understand the construction and working principles of optoelectronic devices
4. Understand the fabrication process of semiconductor devices and CMOS process integration.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method(L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative(Group)Learning in the class.
3. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
4. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real-world and when that's possible, it helps improve the students' understanding.
8. Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.

**Module-1**

**Semiconductors**

Bonding forces in solids, Energy bands, Metals, Semiconductors and Insulators, Direct and Indirect semiconductors, Electrons and Holes, Intrinsic and Extrinsic materials, Conductivity and Mobility, Drift and Resistance, Effects of temperature and doping on mobility, Hall Effect. **(Text1:3.1.1, 3.1.2, 3.1.3, 3.1.4, 3.2.1, 3.2.3, 3.2.4, 3.4.1, 3.4.2, 3.4.3, 3.4.5).**

**Module-2**

**PN Junctions:** Forward and Reverse biased Junctions-Qualitative description of Current flow at a junction, reverse bias, Reverse bias breakdown- Zener breakdown, avalanche breakdown, Rectifiers. **(Text1:5.3.1, 5.3.3, 5.4, 5.4.1, 5.4.2, 5.4.3)** Optoelectronic Devices Photodiodes:

Current and Voltage in an Illuminated Junction, Solar Cells, Photodetectors. Light Emitting Diode: Light Emitting materials.

**(Text1:8.1.1, 8.1.2, 8.1.3, 8.2, 8.2.1),**

**Module-3**

**Bipolar Junction Transistor**

Fundamentals of BJT operation, Amplification with BJTS, BJT Fabrication, the coupled Diode model (Ebers-Moll Model), Switching operation of a transistor, Cutoff, saturation, switching cycle, specifications, Drift in the base region, Base narrowing, Avalanche breakdown.

**(Text1:7.1, 7.2, 7.3, 7.5.1, 7.6, 7.7.1, 7.7.2, 7.7.3)**

**Module-4**

**Field Effect Transistors**

Basic p-n JFET Operation, Equivalent Circuit and Frequency Limitations, MOSFET-Two terminal MO S-structure- Energy band diagram, Ideal Capacitance -Voltage Characteristics and Frequency Effects, Basic MOSFET Operation MOSFET structure, Current-Voltage Characteristics.

**(Text2:9.1.1, 9.4, 9.6.1, 9.6.2, 9.7.1, 9.7.2, 9.8.1, 9.8.2).**

**Module-5**

**Fabrication of p-n junctions**

Thermal Oxidation, Diffusion, Rapid Thermal Processing, Ion implantation, chemical vapour deposition, photolithography, Etching, metallization. **(Text 1: 5.1)**

**Integrated Circuits**

Background, Evolution of ICs, CMOS Process Integration, Integration of Other Circuit Elements. **(Text 1:9.1, 9.2, 9.3.1, 9.3.3).**

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to:

1. Understand the principles of semiconductor Physics
2. Understand the principles and characteristics of different types of semiconductor devices
3. Understand the fabrication process of semiconductor devices
4. Utilize the mathematical models of semiconductor junctions for circuits and systems.
5. Identify the mathematical models of MOS transistors for circuits and systems.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

1. There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
2. Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of

the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks

3. Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based thenonly one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at theend of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
4. The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests andassignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomyas per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers forthe course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximumof 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:Books**


1. Ben. G. Streetman, Sanjay Kumar Banerjee, "Solid State Electronic Devices",7th Edition, PearsonEducation, 2016, ISBN978-93-325-5508-2.
2. Donald A Neamen, Dhrubes Biswas, "Semiconductor Physics and Devices", 4th Edition, McGraw **Hill** Education, 2012, ISBN 978-0-07- 107010-2.


**Reference Books:**


3. S.M. Sze, KwokK.Ng,"PhysicsofSemiconductorDevices",3rd Edition, Wiley,2018.
4. AdirBar-Lev,"SemiconductorandElectronicDevices",3rd Edition, PHI, 1993

| Sensors and Instrumentation | | Semester | 3 |
|---|---|---|---|
| Course Code | 22UEC315C | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

1. Understand various technologies associated in manufacturing of sensors
2. Acquire knowledge about types of sensors used in modern digital systems
3. Get acquainted about material properties required to make sensors
4. Understand types of instrument errors and circuits for multirange Ammeters and Voltmeters.
5. Describe principle of operation of digital measuring instruments and Bridges.
6. Understand the operations of transducers and instrumentation amplifiers.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies; which teacher can use to accelerate the attainment of the various courseoutcomes.

1. Lecture method(L) does not mean only traditional lecture method, but different type ofteaching methods may be adopted to develop the outcomes.
2. Encourage collaborative(Group)Learning in the class.
3. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotescritical thinking.
4. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recallit.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come upwith their own creative ways to solve them.
7. Discuss how every concept can be applied to the real-world and when that's possible, it helpsimprove the students' understanding.
8. Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and
9. have discussions on the topic in the succeeding classes.

**Module-1**

**Introduction to sensor based measurement systems:**

General concepts and terminology, sensor classification, Primary Sensors, material for sensors,
micro sensor technology. (Text 1)

**Module-2**

**Self-generating** Sensors-Thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors. (Text 1)

**Module-3**

**Principles of Measurement:** Static Characteristics, Error in Measurement, Types of Static Error. (Text2: 1.2-1.6)

Multirange Ammeters, Multirange voltmeter. (Text2:3.2,4.4)

**Digital Voltmeter:** Ramp Technique, Dual slope integrating Type DVM, Direct Compensation typeand Successive Approximations type DVM (Text 2: 5.1-5.3, 5.5,5.6)

**Module-4**

**Digital Multimeter:** Digital Frequency Meter and Digital Measurement of Time, Function Generator. **Bridges:** Measurement of resistance: Wheatstone's Bridge, AC Bridges - Capacitance andInductance Comparison bridge, Wien's bridge.
(Text2:refer 6.2,6.3 up to 6.3.2, 6.4 up to 6.4.2, 8.8, 11.2, 11.8 -11.10, 11.14).

**Module-5**

**Transducers:** Introduction, Electrical Transducer, Resistive Transducer, Resistive position Transducer,Resistance Wire Strain Gauges, Resistance Thermometer, Thermistor, LVDT. (Text2:13.1-13.3,13.5, 13.6 up to 13.6.1,13.7,13.8,13.11).

Instrumentation Amplifier using Transducer Bridge, Temperature indicators using Thermometer,Analog Weight Scale(Text2:14.3.3, 14.4.1, 14.4.3).

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to:

1. Understand the material properties required to make sensors
2. Understand the principle of transducers for measuring physical parameters.
3. Describe the manufacturing process of sensors
4. Analyze the instrument characteristics and errors.
5. Describe the principle of operation and develop circuits for multirange Ammeters, Voltmeters and Bridges to measure passive component values and frequency.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

1. There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
2. Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
3. Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then onlyone assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at

the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)

4. The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests andassignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common questionpapers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with amaximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books**


1. "Sensors and Signal Conditioning", Ramon Pallas Areny, JohnG. Webster,2nd edition, John Wiley and Sons,2000
2. H.S.Kalsi, "Electronic Instrumentation", Mc Graw Hill,3rd Edition,2012,ISBN:9780070702066.


**Reference Books**


1. David A. Bell, "Electronic Instrumentation & Measurements", Oxford University Press PHI 2nd Edition, 2006, ISBN 81-203-2360-2.
2. D. HelfrickandW.D. Cooper, "Modern Electronic Instrumentation and MeasuringTechniques", Pearson, 1stEdition, 2015, ISBN: 9789332556065.


**Web links and Video Lectures (e-Resources):**

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

| Computer Organization and Architecture | | Semester | 3 |
|---|---|---|---|
| Course Code | 22UEC315B | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type (SEE) | Theory | | |

**Course objectives:** This course will enable students to:

1. Explain the basic sub systems of a computer, their organization, structure and operation.
2. Illustrate the concept of programs as sequences of machine instructions.
3. Demonstrate different ways of communicating with I/O devices
4. Describe memory hierarchy and concept of virtual memory.
5. Illustrate organization of simple pipelined processor and other computing systems.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative (Group) Learning in the class.
3. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
4. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world-and when that's possible,it helps improve the students' understanding.
8. Adopt Flipped class technique by sharing the materials/Sample Videos prior to the class and have discussions on the topic in the succeeding classes.

**Module-1**

**Basic Structure of Computers:** Computer Types, Functional Units, Basic Operational Concepts, Bus Structures, Software, Performance -Processor Clock, Basic Performance Equation**(upto1.6.2ofChap1ofText).**

**Machine Instructions and Programs:** Numbers, Arithmetic Operations and Characters, IEEE standard for Floating Point Numbers, Memory Location and Addresses, Memory Operations, Instructions and Instruction Sequencing **(up to 2.4.6 of Chap 2 and 6.7.1 of Chap 6 of Text).**

**Module-2**

Addressing Modes, Assembly Language, Basic Input and Output Operations, Stacks andQueues, Subroutines, Additional Instructions **(from 2.4.7 of Chap2, except 2.9.3, 2.11 & 2.12 of Text).**

**Module-3**

**Input/ Output Organization:** Accessing I/O Devices, Interrupts -Interrupt Hardware, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling Device Requests, Direct Memory Access
(up to 4.2.4 and 4.4 except 4.4.1of Chap 4 of Text).

**Module-4**

**Memory System:** Basic Concepts, Semiconductor RAM Memories-Internal organization of memory chips, Static memories, Asynchronous DRAMS, Read Only Memories, Cash Memories, Virtual Memories, Secondary Storage Magnetic Hard Disks **(5.1, 5.2, 5.2.1, 5.2.2, 5.2.3, 5.3, 5.5 (except 5.5.1 to** 5.5.4), 5.7 (except5.7.1), 5.9, 5.9.1 of Chap 5 of Text).

**Module-5**

**Basic Processing Unit:** Some Fundamental Concepts, Execution of a Complete Instruction, Multiple Bus Organization, Hardwired Control, Microprogrammed Control **(up to 7.5 except 7.5.1 to7.5.6 of Chap 7 of Text).**

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to:

1. Explain the basic organization of a computer system.
2. Describe the addressing modes, instruction formats and program control statement.
3. Explain different ways of accessing an input/ output device including interrupts.
4. Illustrate the organization of different types of semiconductor and other secondary storage memories.
5. Illustrate simple processor organization based on hard wired control and micro-Programmed control.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE(Semester End Examination) taken together.

**Continuous Internal Evaluation:**

1. There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
2. Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks

3. Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments atthe end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall bescaled down to 25 marks)
4. The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.

There will be 2 questions from each module. Each of the two questions under a module (witha maximum of 3 sub-questions), **should have a mix of topics** under that module.

**Suggested Learning Resources:**

**Book**

1. Carl Hamacher, Zvonko Vranesic, Safwat Zaky: Computer Organization, 5th Edition, Tata McGrawHill,2002.

**Reference Books:**

2. David A. Patterson, John L. Hennessy: Computer Organization and Design-The Hardware/ Software Interface ARM Edition, 4th Edition, Elsevier,2009.
3. William Stallings: Computer Organization &Architecture,7th Edition, PHI, 2006.
4. Vincent P. Heuring & Harry F. Jordan: Computer Systems Design and Architecture, 2nd Edition, Pearson Education, 2004.

**Web links and Video Lectures (e-Resources):**

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

| Course Outcomes | Pos | | | | | | | | | | | | PSOs | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | a | b | c | d | E | f | g | h | i | J | k | l | m | n | O |
| **CO1:** Explain the basic organization of a computer system. | 2 | 2 | 2 | 1 | 2 | - | - | - | - | - | 2 | 1 | 2 | - | 2 |
| **CO2:** Describe the addressing modes, instruction formats and program control statement. | 3 | 2 | 1 | 1 | 1 | - | - | - | - | - | 2 | 1 | 1 | 1 | 2 |
| **CO3:** Explain different ways of accessing an input/output device including interrupts. | 2 | 1 | 2 | 1 | 1 | - | - | - | - | - | 2 | 1 | 2 | 1 | 1 |
| **CO4:** Illustrate the organization of different types of semiconductor and other secondarystorage memories | 1 | 2 | 3 | 1 | 3 | 1 | - | - | - | - | 2 | 1 | 2 | 1 | - |
| **CO5:** Illustrate simple processor organization based on hard wired control and micro-programmed control. | 1 | 2 | 2 | 1 | 2 | - | - | - | - | - | 2 | 1 | 3 | - | 1 |
| **Course Contribution to POs** | **1.8** | **1.8** | **2** | **1** | **1.8** | **1** | | | | | **2** | **1** | **2** | **1** | **1.5** |

| Applied Numerical Methods for EC Engineers | | Semester | 3 |
|---|---|---|---|
| Course Code | 22UEC315D | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |
| Examination type (SEE) | **Theory** | | |

**Course objectives:**

1. To provide the knowledge and importance of error analysis in engineering problems
2. To represent and solve an application problem using a system of linear equations
3. Analyze regression **data** to choose the most appropriate model for a situation.
4. Familiarize with the ways of solving complicated mathematical problems numerically
5. Prepare **to solve** mathematical models represented by initial or boundary value problems

**Teaching-Learning Process Pedagogy**
**(General Instructions):**

These are sample Strategies, teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills.
2. State the need for Mathematics with Engineering Studies and Provide real-life examples.
3. Support and guide the students for self–study.
4. You will assign homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students to group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
    i. As an introduction to new topics (pre-lecture activity).
    ii. As a revision of topics (post-lecture activity).
    iii. As additional examples (post-lecture activity).
    iv. As an additional material of challenging topics (pre-and post-lecture activity).
    v. As a model solution of some exercises (post-lecture activity).

**Module-1: Errors in computations and Root of the equations**

Approximations and Round Off -Errors in computation: Error definitions, Round-Off errors, Truncation errors and the Taylor series-The Taylor series, Error Propagation, Total numerical error, Absolute, Relative and percentage errors, Blunders, Formulation errors and data uncertainty. Roots of equations: Simple fixed point iteration methods. Secant Method, Muller's method, and Graeffe's Roots Squaring Method. Aitkin's Method. **(8 hours)**

**Module-2: Solution of System of Linear Equations**

Rank of the matrix, Echelon form, Linearly dependent and independent equations, Solutions for linear equations, Partition method, Croute's Triangularisation method. Relaxation method. Solution of non-linear simultaneous equations by Newton-Raphson method. Eigen Values and properties, Eigen Vectors, Bounds on Eigen Values, Jacobi's method, Given's method for symmetric matrices. **(8 hours)**

**Module-3: Curve Fitting**

Least-Squares Regression: Linear Regressions, Polynomial regressions, Multiple Linear regressions, General Linear Least squares, Nonlinear Regressions, QR Factorization. Curve Fitting with Sinusoidal Functions

Introduction to Splines, Linear Splines, Quadratic Splines, Cubic Splines. Bilinear Interpolation. **(8 hours)**

**Module-4:**
**Numerical integration, Difference equations and Boundary Value Problems**

Romberg's method, Euler-Maclaurin formula, Gaussian integration for n = 2 and n=3. Numerical double integration by trapezoidal and Simpson's 1/3 rd rule. Solution of linear difference equations.

Boundary-Value Problems, Introduction. The Shooting Method, Finite-Difference Methods. **(8 hours)**

**Module-5:**
**Numerical solution of partial differential equations**

Classifications of second-order partial differential equations, Finite difference approximations to partial derivatives. Solution of: Laplace equation, Poisson equations, one-dimensional heat equation and wave equations. **(8 hours)**

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to:

1. Explain and measure errors in numerical computations
2. Test for consistency and solve a system of linear equations.
3. Construct a function which closely fits given n- n-points of an unknown function.
4. Understand and apply the basic concepts related to solving problems by numerical differentiation and numerical integration.
5. Use appropriate numerical methods to study phenomena modelled as partial differential equations.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20marks out of 50) and for the SEE, the minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the **CIE** (Continuous Internal Evaluation) and **SEE** (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

1. There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
2. Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks

3. Any two assignment methods mentioned in the 22OB2.4, if an assignment is project- based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
4. The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**The Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Books (Name of the author/Title of the Book/Name of the publisher/Edition and Year)Text Books:**


1. **Steven C. Chapra & Raymond P. Canale: "**Numerical Methods for Engineers and Scientists", McGraw Hill, 8th Edition, 2020.
2. **Steven C. Chapra**: "Applied Numerical Methods with MATLAB for Engineers and Scientists", McGraw Hill, Fifth Edition, 2023.
3. **B. S. Grewal**: "Numerical Methods in Engineering & Science with programs in C, C++and MATLAB", Khanna Publishers, 10hEd., 2015.


**Reference Books:**


1. **John H. Mathews & Kurtis D. Frank**: "Numerical Methods Using MATLAB", PHI Publications, 4th Edition, 2005.

**Won Young Yang, Wenwu Cao, Tae Sang Chung, John Morris: "**Applied Numerical Methods Using MATLAB**",** WILEY Inter science**,** Latest Edition, 2005.


**Activity-Based Learning (Suggested Activities in Class)/Practical-Based Learning**

- Quizzes
- Assignments
- Seminar

| Lab VIEW Programming | | Semester | 3 |
|---|---|---|---|
| Course Code | 22UEC316D | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 0:0:2 | SEE Marks | 50 |
| Credits | 01 | Total | 100 |
| | | Exam Hours | 2 |
| Examination type (SEE) | Practical | | |

**Course objectives:**

1. Aware of various front panel controls and indicators.
2. Connect and manipulate nodes and wires in the block diagram.
3. Locate various tool bars and pull-down menus for the purpose of implementing specific functions.
4. Locate and utilize the context help window.
5. Familiar with LabVIEW and different applications using it.

| Sl. NO | VI Programs(using LabVIEW software)to realize the following: |
|---|---|
| 1 | Basic arithmetic operations: addition, subtraction, multiplication and division |
| 2 | Boolean operations: AND, OR, XOR, NOT and NAND |
| 3 | Sum of ‘n’ numbers using ‘for’ loop |
| 4 | Factorial of a given number using ‘for’ loop |
| 5 | Determine square of a given number |
| 6 | Factorial of a given number using ‘while‘ loop |
| 7 | Sorting even numbers using ‘while’ loop in an array |
| 8 | Finding the array maximum and array minimum |
| | Demonstration Experiments (For CIE) |
| 9 | Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically. |
| 10 | Build a Virtual Instrument that simulates a Basic Calculator (using formula node). |
| 11 | Build a Virtual Instrument that simulates a Water Level Detector. |
| 12 | DemonstratehowtocreateabasicVIwhichcalculatestheareaandperimeterofacircle. |

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

1. Use LabVIEW to create data acquisition, analysis and display operations
2. Create user interfaces with charts, graph and buttons
3. Use the programming structures and data types that exist in LabVIEW
4. Use various editing and debugging techniques.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between

the schedule mentioned in the academic calendar of the University.

- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

**Suggested Learning Resources:**

1. Virtual Instrumentation using LABVIEW, Jovitha Jerome, PHI,2011
Virtual Instrumentation using LABVIEW, Sanjay Gupta, Joseph John, TMH, McGraw-Hill, Second Edition, 2011.

| MATLAB Programming | | Semester | 3 |
|---|---|---|---|
| Course Code | 22UEC316C | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 1:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 14 | Total Marks | 100 |
| Credits | 01 | Exam Hours | 1 |
| Examination type (SEE) | Theory | | |

**Course objectives:**

- Understand the MATLAB commands and functions.
- Create and Execute the script and function files
- Work with built in function, saving and loading data and create plots.
- Work with the arrays, matrices, symbolic computations, files and directories.
- Learn MATLAB programming with script, functions and language specific features.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Adopt Problem Based Learning (PBL), which fosters students' analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
2. Give programming assignments.

**Module-1**

**Introduction:** Basics of MATLAB, Simple arithmetic calculations, Creating and working with arrays and numbers.

**Module-2**

Creating and printing simple plots, Creating, saving and executing a script file, Creating and executing a function file, Working with arrays and matrices.

**Module-3**

Working with anonymous functions, Symbolic Computations, Importing and exporting data, Working with files and directories.

**Module-4**

**Interactive computations:** Matrices and vectors, Matrix and array operations, Character strings, Command line functions, Built-in functions, Saving and loading data, Plotting simple plots.

**Module-5**

**Programming in MATLAB:** Script Files, Function Files, Language specific Features.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to:

1. Understand the syntax of MATLAB for arithmetic computations, arrays, matrices.
2. Understand the built in function, saving and loading data, and create plots
3. Create program using symbolic computations, Importing and exporting data and files
4. Create program using character strings, Command line functions and Built-in functions.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

**Continuous internal Examination (CIE)**

1. For the Assignment component of the CIE, there are 25 marks and for the Internal AssessmentTest component, there are 25 marks.
2. The first test will be administered after 40-50% of the syllabus has been covered, and the secondtest will be administered after 85-90% of the syllabus has been covered
3. Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based thenonly one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
4. For the course, CIE marks will be based on a scaled-down sum of two tests and other methods ofassessment.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomyas per the outcome defined for the course.**

**Semester End Examinations (SEE)**

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to secure a minimum of 35% of the maximum marks meant for SEE.

OR

MCQ (Multiple Choice Questions) are preferred for 01 credit courses, however, if course content demands the general question paper pattern that followed for 03 credit course, then

1. The question paper will have ten questions. Each question is set for 10 marks.
2. There will be 2 questions from each module. Each of the two questions under a module may or may nothave the sub-questions (with maximum sub-questions of 02, with marks distributions 5+5, 4+6, 3+7).
3. The students have to answer 5 full questions, selecting one full question from each module.
4. **The duration of the examinations shall be defined by the concerned board of studies**

**Suggested Learning Resources: Book**

1. Rudra Pratap, Getting Started with MATLAB – A quick Introduction for scientists and Engineers, Oxford University Press, 2010.

**Web links and Video Lectures (e-Resources):**

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

| C++ Basics | | Semester | 4 |
|---|---|---|---|
| Course Code | 22UEC316A | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | 0:0:2:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 24 | Total Marks | 100 |
| Credits | 1 | Exam Hours | 02 |
| Examination nature (SEE) | Practical | | |

**Course objectives:**

- Understand object-oriented programming concepts, and apply them in solving problems.
- To create, debug and run simple C++ programs.
- Introduce the concepts of functions, friend functions, inheritance, polymorphism and function overloading.
- Introduce the concepts of exception handling and multithreading.

| Sl. No | Experiments |
|---|---|
| 1 | Write a C++ program to find largest, smallest & second largest of three numbers using inline functions MAX & Min. |
| 2 | Write a C++ program to calculate the volume of different geometric shapes like cube, cylinder and sphere using function overloading concept. |
| 3 | Define a STUDENT class with USN, Name & Marks in 3 tests of a subject. Declare an array of 10<br>STUDENT objects. Using appropriate functions, find the average of the two better marks for each student. Print the USN, Name & the average marks of all the students. |
| 4 | Write a C++ program to create class called MATRIX using two-dimensional array of integers, by overloading the operator == which checks the compatibility of two matrices to be added and subtracted. Perform the addition and subtraction by overloading + and – operators respectively. Display the results by overloading the operator <<. If (m1 == m2) then m3 = m1 +<br>m2 and m4 = m1 – m2 else display error |
| 5 | Demonstrate simple inheritance concept by creating a base class FATHER with data members: *First Name, Surname, DOB & bank Balance* and creating a derived class SON, which inherits: Surname & Bank Balance feature from base class but provides its own feature: First Name & DOB. Create & initialize F1 & S1 objects with appropriate constructors & display the FATHER & SON<br>details. |
| 6 | Write a C++ program to define class name FATHER & SON that holds the income respectively. Calculate & display total income of a family using Friend function. |
| 7 | Write a C++ program to accept the student detail such as name & 3 different marks by get_data () method & display the name & average of marks using display () method. Define a friend function for calculating the average marks using the method mark_avg (). |
| 8 | Write a C++ program to explain virtual function (Polymorphism) by creating a base class polygon which has virtual function areas two classes rectangle & triangle derived from polygon & they have area to calculate & return the area of rectangle & triangle respectively. |

| | |
|---|---|
| 9 | Design, develop and execute a program in C++ based on the following requirements: An EMPLOYEE class containing data members & members functions: i) Data members: employee number (an integer), Employee_ Name (a string of characters), Basic_ Salary (in integer), All_ Allowances (an integer), Net_Salary (an integer). (ii) Member functions: To read the data of an employee, to calculate Net_Salary & to print the values of all the data members. (All_Allowances = 123% of Basic, Income Tax (IT) =30% of gross salary (=basic_ Salary_All_Allowances_IT). |
| 10 | Write a C++ program with different class related through multiple inheritance & demonstrate the use of different access specified by means of members variables & members functions. |
| 11 | Write a C++ program to create three objects for a class named count object with data members |
| | such as roll no & Name. Create a members function set data () for setting the data values & display ( ) member function to display which object has invoked it using „this" pointer. |
| 12 | Write a C++ program to implement exception handling with minimum 5 exceptions classes including two built in exceptions. |

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

1. Write C++ program to solve simple and complex problems
2. Apply and implement major object-oriented concepts like message passing, function overloading, operator overloading and inheritance to solve real-world problems.
3. Use major C++ features such as Templates for data type independent designs and File I/O to deal with large data set.
4. Analyze, design and develop solutions to real-world problems applying OOP concepts of C++

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the $8^{th}$ week of the semester and the second test shall be conducted after the $14^{th}$ week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.

Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero.

The duration of SEE is 03 hours Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**


1. Object oriented programming in TURBO C++, Robert Lafore, Galgotia Publications, 2002
2. The Complete Reference C++, Herbert Schildt, 4th Edition, Tata McGraw Hill, 2003.
3. Object Oriented Programming with C++, E Balaguruswamy, 4th Edition, Tata McGraw Hill, 2006.

| IoT for Smart Infrastructure | | Semester | 3 |
|---|---|---|---|
| Course Code | 22UEC316B | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | 1:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 14 | Total Marks | 100 |
| Credits | 01 | Exam Hours | 1 |
| Examination type (SEE) | Theory/Practical | | |

**Course objectives:**

To provide an understanding of the concepts, principles, and applications of IoT in the context of smart infrastructure.

To explore the role of IoT technologies in transforming infrastructure into smart, efficient, and sustainable systems and analyze the challenges, opportunities, and considerations in implementingIoT for smart infrastructure.

To examine real-world case studies and successful implementations of IoT in smart cities, buildings, transportation, and energy management and explore future trends and emerging technologies shaping the field of IoT for smart infrastructure.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

- **Interactive Lectures:** Conduct interactive lectures to present the theoretical concepts and foundational knowledge of IoT for smart infrastructure.
- **Case Studies and Group Discussions:** Utilize case studies to analyze real-world implementations of IoT in smart infrastructure projects. Divide students into groups and assign them specific cases to discuss and analyze.
- **Hands-on Workshops and Simulations:** Organize hands-on workshops or simulations where students can interact with IoT devices and technologies relevant to smart infrastructure.
- **Guest Lectures and Industry Experts:** Invite guest speakers or industry experts who have hands-on experience in implementing IoT in smart infrastructure projects. They can share their insights, challenges, and success stories, providing students with a real-world perspective
- **Project-Based Learning:** Assign students to work on individual or group projects relatedto IoT for smart infrastructure. Provide a project brief with specific objectives and deliverables. Students can apply their knowledge and skills to design, develop, or analyze IoT solutions for smart infrastructure challenges.

**Module-1**

**Introduction to IoT and Smart Infrastructure**

Introduction to IoT: Definition of IoT and its basic components, Overview of IoT applications in various industries, Importance of IoT in transforming infrastructure.

Smart Infrastructure Overview: Introduction to smart infrastructure and its key components, Benefits and challenges of implementing smart infrastructure, Case studies showcasing successful smart infrastructure projects.

IoT Technologies for Smart Infrastructure: Sensors and actuators: Types, functionalities, and applications; Communication protocols: Wi-Fi, Bluetooth, cellular networks, and their use in IoT;

Cloud computing and data analytics in IoT for infrastructure; Edge computing: Real-time decision-making at the edge. Security and Privacy in IoT for Smart Infrastructure: Security challenges and threats in IoT, Privacy considerations and data protection in smart infrastructure, best practices and solutions for ensuring IoT security and privacy.

**Module-2**

**IoT Applications in Smart Cities**

Introduction to Smart Cities - Definition and key features of smart cities, Role of IoT in transforming cities into smart cities, Benefits and challenges of smart city implementations. IoT Applications in Smart City Infrastructure - Smart transportation: Intelligent traffic management and transportation systems, Smart buildings: Energy management and occupant comfort; Smart grids: Optimizing energy distribution and consumption; Waste management, water management, and environmental monitoring. Case Studies of Smart City Implementations: Showcase of successful smart city projects around the world; Analysis of the IoT technologies and strategies implemented; Lessons learned from these case studies. Future Trends in Smart Cities: Emerging technologies shaping the future of smart cities, Role of IoT, AI, and 5G in advancing smart city infrastructure, Opportunities and challenges for future smart city developments.

**Module-3**

**IoT Applications in Smart Buildings**

Introduction to Smart Buildings: Definition and key features of smart buildings, Benefits of IoTin improving energy efficiency and occupant comfort, Challenges and considerations in implementing smart building technologies. IoT Technologies for Smart Buildings: Building automation systems and controls; Energy management and monitoring using IoT devices; Indoor environmental quality monitoring and optimization; Smart lighting and HVAC systems. Case Studies of Smart Building Implementations: Showcase of successful smart building projects; Analysis of IoT technologies and solutions deployed; Lessons learned from these case studies. Future Trends in Smart Buildings: Emerging technologies for smart buildings; Integration of IoT with AI and machine learning; Potential impact of 5G on smart building applications.

**Module-4**

**IoT Applications in Smart Transportation**

Introduction to Smart Transportation: Definition and key features of smart transportation; Role of IoT in intelligent traffic management and transportation systems; Challenges and opportunities in implementing smart transportation solutions. IoT Technologies for Smart Transportation: Traffic sensors and monitoring systems; Intelligent transportation systems (ITS); Vehicle-to-vehicle (V2V) and vehicle-to-infrastructure (V2I) communication; Real-time data analysis and predictive analytics.

Case Studies of Smart Transportation Implementations: Showcase of successful smart transportation projects; Analysis of IoT technologies and solutions deployed; Lessons learned from these case studies.

Future Trends in Smart Transportation: Emerging technologies shaping the future of smart transportation; Role of IoT, AI, and autonomous vehicles; Potential impact of 5G on smart transportation applications.

**Module-5**

**IoT for Smart Grids and Energy Management**

Introduction to Smart Grids: Definition and key features of smart grids: Role of IoT in optimizing energy distribution and consumption; Benefits and challenges of smart grid implementations. IoT Technologies for Smart Grids: Smart meters and energy monitoring devices; Demand response and load management; Grid optimization and fault detection using IoT; Renewable energy integration and grid stability. Case Studies of Smart Grid Implementations: Showcase of successful smart grid projects, Analysis of IoT technologies and solutions deployed, Lessons learned from these case studies. Future Trends in Smart Grids and Energy Management: Emerging technologies for smart grids;Integration of IoT, AI, and block chain in energy management; Potential impact of 5G on smartgrid applications.

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to:

- Define and explain the core concepts and components of IoT and its relevance to smart infrastructure. Identify and evaluate the key technologies and communication protocols used in IoT for smart infrastructure.
- Assess the benefits, challenges, and ethical considerations associated with implementing IoT in smart infrastructure projects and analyze & compare different IoT applications in smart cities, buildings, transportation, and energy management.
- Examine real-world case studies of successful IoT implementations in smart infrastructure and extract lessons learned. Demonstrate an understanding of security and privacy considerations in IoT for smart infrastructure.
- Discuss the impact of emerging technologies, such as artificial intelligence and 5G, on the future of IoT in smart infrastructure. Apply knowledge and critical thinking skills to propose IoT-based solutions for smart infrastructure challenges.
- Work effectively in teams to analyze, design, and present IoT projects related to smart

infrastructure and communicate effectively and articulate the potential benefits and limitations of IoT for smart infrastructure.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous internal Examination (CIE)**

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examinations (SEE)**

SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions). The time allotted for SEE is **01 hour.** The student has to secure a minimum of 35% of the maximum marks meant for SEE.

**Web links and Video Lectures (e-Resources):** makes.mindmatrix.io

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

1. Sensor Deployment and Data Collection: Organize a hands-on activity where participants work in groups to deploy sensors in a simulated smart infrastructure environment.
2. Smart City Simulation Game: Develop a simulation game where participants take on different roles representing stakeholders in a smart city.
3. IoT Solution Design Challenge: Assign participants to design an IoT-based solution for a specific smart infrastructure problem. They can work individually or in teams to identify the problem, propose an IoT solution, outline the required components and technologies, and create a prototype or presentation.
4. Security and Privacy Risk Assessment: Conduct a group activity where participants analyse the security and privacy risks associated with IoT deployments in smart infrastructure.

Field Visit to Smart Infrastructure Project: Organize a field visit to a smart infrastructure project, such as a smart building, smart city district, or IoT-enabled transportation system.

| SOCIAL CONNECT & RESPONSIBILITIES | | | |
|---|---|---|---|
| **Course Code** | **21SCR36** | **CIE Marks** | **50** |
| Teaching Hours week (L:T:P:S) | 1: 0: 0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 15 | Total Marks | 100 |
| Credits | 01 | Exam Hours | 03 |
| Department | Management Studies / Engineering Department | | |
| Offered for | 3rd Semester | | |
| Prerequisite | Nil | | |
| | | | |

**Objectives:** The Course will

- Enable the student to do a deep drive into societal challenges being addressed by NGO(s), social enterprises & The government and build solutions to alleviate these complex social problems through immersion, design & technology.
- Provide a formal platform for students to communicate and connect with their surroundings.
- Enable to create of a responsible connection with society.

**Learning Outcomes:** The students are expected to have the ability to :

1. Understand social responsibility
2. Practice sustainability and creativity
3. Showcase planning and organizational skills

**Contents:**

The course is mainly activity-based that will offer a set of activities for the student that enables them to connect with fellow human beings, nature, society, and the world at large. The course will engage studentsinr interactive sessions, open mic, reading groups, storytelling sessions, and semester-long activities conducted by faculty mentors. In the following a set of activities planned for the course have been listed :

**Module-I**

**Plantation and adoption of a tree:** Plantation of a tree that will be adopted for four years by a group of B.Tech. students. They will also make an excerpt either as a documentary or a photoblog describing the plant's origin, its usage in daily life, and its appearance in folklore and literature.

**Module-II**

**Heritage walk and crafts corner:** Heritage tour, knowing the history and culture of the city, connecting to people around through their history, knowing the city and its craftsman, photoblog and documentary on evolution and practice of various craft forms.

**Module-III**

**Organic farming and waste management:** usefulness of organic farming, wet waste managementin neighboring villages, and implementation in the campus.

**Module-IV**

**Water Conservation:** knowing the present practices in the surrounding villages and

implementation in the campus, documentary or photo blog presenting the current practices.

**Module-V**

**Food Walk** City's culinary practices, food lore, and indigenous materials of the region used in cooking.

**Activities**

**Jamming session, open mic, and poetry:** Platform to connect to others. Share the stories with others. **Share the experience of Social Connect**. Exhibit the talent like playing instruments, singing, one-act play, art-painting, and fine art.

**PEDAGOGY**

The pedagogy will include interactive lectures, inspiring guest talks, field visits, social immersion, and a course project. Applying and synthesizing information from these sources to define the social problem to address and take up the solution as the course project, with your group. Social immersionwith NGOs/social sections will be a key part of the course. Will all lead to the course project that will address the needs of the social sector?

**COURSE TOPICS:**

The course will introduce social context and various players in the social space, and present approaches to discovering and understanding social needs. Social immersion and inspiring conversional will culminate in developing an actual, idea for problem-based intervention, based on an in-depth understanding of a key social problem.

A total of 14-20 hrs engagement per semester is required for the 3rd semester of the B.E. /B.Tech. program. The students will be divided into 10 groups of 35 each. Each group will be handled by two **faculty mentors**. Faculty mentors will design the activities (particularly Jammingsessions open mic ,and poetry)

**Faculty mentors** has to design the evaluation system.

| **Course Outcomes** | **Pos** | | | | | | | | | | | | **PSOs** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **a** | **b** | **c** | **d** | **e** | **f** | **g** | **H** | **i** | **J** | **k** | **l** | **m** | **n** | **o** |
| **CO1:** Understand social responsibility | - | - | - | - | - | - | 2 | 1 | 3 | 3 | - | 3 | - | - | - |
| **CO2:** Understand Indian culture and history | - | - | - | - | - | - | 2 | - | 1 | 3 | - | 3 | - | - | - |
| **CO3:** Understand smart agriculture | - | - | - | 1 | - | 3 | 3 | - | 2 | 3 | 3 | 3 | - | - | - |
| **CO4:** Practice sustainability and creativity | - | - | - | - | - | 3 | 2 | 2 | 2 | 3 | 2 | 3 | - | - | - |
| **CO5:** Showcase planning and organizational skills | - | - | - | - | - | 1 | 1 | - | 2 | 3 | - | 3 | - | - | - |
| **Course Contribution to POs** | **-** | **-** | **-** | **1** | **-** | **2.3** | **2** | **1.5** | **2** | **3** | **2.5** | **3** | **-** | **-** | **-** |

**Guideline forAssessment Process:**

**Continuous Internal Evaluation (CIE)**

After completion of, the social connect, the student shall prepare, with daily **diary** as reference, a comprehensive report in consultation with the mentor/s to indicate what he has observed and learned in the social connect period. The report should be signed by the mentor. The report shall be evaluated on the basis of the following criteria and/or other relevant criteria pertaining to the activity completed.

Marks allotted for the diary are out of 50.

Planning and scheduling the social connect

Information/Data collected during the social connect

Analysis of the information/data and report writing

Considering all above points allotting the marks as mentioned below-

**Semester End Examination (SEE)**

This Jamming session will be conducted at the end of the course for **50 marks**

Jamming session includes -Platform to connect to others. Share the stories with others. **Share the experience of Social Connect**. Exhibit the talent like playing instruments, singing, one-act play, art painting, and fine art.

Faculty mentor has to design the evaluation system for the Jamming session.

| | |
|---|---|
| Excellent | 80 to 100 |
| Good | 60 to 79 |
| Satisfactory | 40 to 59 |
| Unsatisfactoryand fail | <39 |

## Pedagogy (Guidelines) may differ depending on local resources available for the study

| Module | Topic | Content | Group Size | Location | Magnitude | Activity | Reporting | Evaluation |
|---|---|---|---|---|---|---|---|---|
| I | Plantation and adoption ofa tree | Plantation of a tree that will be adopted for four years by a group of B.Tech. students. They will also make an excerpt either as a documentary or a photoblog describing the plant's origin, its usage in daily life, and its appearance in folklore and literature. | 03 – 05 | Farmers Land or Road side or Community area or institution's campus, any one location to be selected. | One<br><br>Students must monitor itfor three years | Site selection<br><br>Select suitable species in consultation with horticulture, forest or agriculture department. Interact with NGO/Industry and community to plant Tag the plant for continuous monitoring | Report shall be hand writtenn or blog with paintings, sketches, poster, video and/or photograph with Geo tag. | Each module is evaluated for 50 Marks and average of all the five modules will be the final marks.<br><br>**CIE Rubrics for 50 M**<br><br>Planning and scheduling the social connect – 15 M<br><br>Information/Data collected during the social connect – 15 M<br><br>Analysis of the information/data and report writing – 20 M<br><br>**SEE 50 M:** Presentation, Jamming session, Open mic, Group |
| II | Heritage walk and crafts corner | Heritage tour, knowing the history and culture of the city, connecting to people around through their history, knowing the city and its craftsman, photoblog and documentary on evolution and practice of various craft forms. | 03 - 05 | Preferably Within the city where institution is located or home town of the student group | One or two<br><br>One can be a structure or a heritage building theother can be heritage custom or practise | Survey in the form of questioner by connecting to the people and asking. No standard questioner to be given by faculty and has to be evolved involving students. Questions during survey can be asked in local language but report language is English. | | |
| III | Waste management | Wet waste management in neighbouring villages, and implementation in the campus. | 03 - 05<br><br>More than one group can be | Preferably in the nearby villages and within the campus. | One | Report on importance and benefits of Waste management. Report on segregation, collection, transportation and disposal. | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | assigne d one task based on magnitude of task. | | | Suggestion for composting.<br>Visit nearby village/location to sensitize farmers andpublic about waste management and also document current practises. | | discussion and debate. |
| III | Organic farming | Usefulness of organic farming in neighbouring villages, and implementationin the campus. | 03 – 05 | Visit to farming lands where organic farming is going on<br><br>Campus Garden<br><br>Roof top Garden or Vertical Garden or hydroponics if land is scarce. | One | Collect data on organic farming in the vicinity.Like types of crop, methodology etc.,.<br><br>Suggestion for implementation at selected locations | | |
| IV | Water Conservati on | Knowing the present practices in the surroundingvillages and implementationin the campus, documentaryor photo blog presenting thecurrent practices. | 03 – 05 | Rain water harvesting demonstration available in the campus or surroundings | One | Visit lakes/pond/river/dry well to involve on rejuvenation activity.<br><br>Or<br><br>Assessment of Water budget in the campus/village | | |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Report on traditional water conservation practices (to minimize wastage) | | |
| V | Food Walk | City's culinary practices, food lore, and indigenous materials of the region used in cooking. | 03 - 05 | Within the city where institution is located<br><br>Food culture of student's resident region | One | Survey local food centres and identify the speciality<br><br>Identify and study the food ingredients<br><br>Report on the regional foods<br><br>Report on Medicinals values of the local food grains, and plants. | | |

**Important recommendations requested; Special Appreciation from institution and university for students who take care of plants for three years.

# IV Sem Syllabus

| ELECTROMAGNETIC THEORY | | Semester | IV |
|---|---|---|---|
| Course Code | **22UEC410C** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |
| Examination type (SEE) | THEORY | | |

**Course objectives:**

This course will enable students to:

1. Study the different coordinate systems, Physical significance of Divergence, Curl and Gradient.
2. Understand the applications of Coulomb's law and Gauss law to different charge distributions and the applications of Laplace's and Poisson's Equations to solve real time problems on capacitance of different charge distributions.
3. Understand the physical significance of Biot-Savart's, Ampere's Law and Stokes' theorem for different current distributions.
4. Infer the effects of magnetic forces, materials and inductance.
5. Know the physical interpretation of Maxwell's equations and applications for Plane waves for their behavior in different media.
6. Acquire knowledge of Poynting theorem and its application of power flow

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes. These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different types of teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative (Group) Learning in the class.
3. Ask at least three HOTS (Higher Order Thinking) questions in the class, which promotes critical thinking.
4. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up with creative ways to solve them.
7. Discus show every concept can be applied to the real world and when that's possible, it helps improve the student's understanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class andhaving discussions on the topic in the succeeding classes.

**Module-1**

Revision of Vector Calculus – **(Text 1: Chapter 1)**
**Coulomb's Law, Electric Field Intensity and Flux density**: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge, Field due to Sheet of charge, Electric flux density, Numerical Problems.
**(Text: Chapter 2.1 to 2.5, 3.1)**

**Module-2**

**Gauss's Law and Divergence**: Gauss 'law, Application of Gauss' law to Point Charge, line charge, Surface charge and Volume Charge, Point (differential) form of Gauss law, Divergence. Maxwell's First Equation (Electrostatics), Vector Operator ▼and divergence theorem, Numerical Problems (**Text: Chapter 3.2 to 3.7).**Energy expended or work done in moving a point charge in an Electric field, The line integral (**(Text: Chapter 4.1 and 4.2)** Current and Current density, Continuity of current. **(Text: Chapter 5.1, 5.2)**

**Module-3**

**Poisson's and Laplace's Equations**: Derivation of Poisson's and Laplace's Equations, Examples of the solution of Laplace's equation, Numerical problems on Laplace's equation
**(Text: Chapters 7.1 and 7.3)**
**Steady Magnetic Field**: Biot-Savart Law, Ampere's circuital law, Curl, Stokes' theorem,Magnetic flux and magnetic flux density.
(**Text: Chapters 8.1 to 8.5)**

**Module-4**

**Magnetic Forces**: Force on a moving charge, differential current elements, Force between differential current elements, Numerical problems **(Text: Chapter 9.1 to 9.3).**
**Magnetic Materials**: Magnetization and permeability, Magnetic boundary conditions, the magnetic circuit, problems **(Text: Chapter 9.6 to 9.8)**

**Module-5**

Faraday's law of Electromagnetic Induction –Integral form and Point form, Numerical problems. Inconsistency of Ampere's law with continuity equation, displacement current, Conduction current, Derivation of Maxwell's equations in point form, and integral form, Maxwell's equations for different media, Numerical problems **(Text: Chapter 10.1 to 10.4)**
**Uniform Plane Wave**: Wave propagation in free space, Uniform plane wave, Derivation of plane wave equations from Maxwell's equations, Poynting's Theorem and wave power, Skin effect or Depth of penetration, Numerical problems. **(Text: Chapter 12.1, 12.3, 12.4)**

**Course outcome (Course Skill Set)**

At the end of the course the student will be able to:

1. Evaluate problems on electrostatic force, electric field due to point, linear, volume charges by applying conventional methods and charge in a volume.
2. Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution by using Divergence Theorem.
3. Determine potential and energy with respect to point charge and capacitance using Laplace equation and Apply Biot-Savart's and Ampere's laws for evaluating Magnetic field for different current configurations
4. Calculate magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits.
5. Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and Evaluate power associated with EM waves using Poynting theorem

**ssessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

1. There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
2. Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
3. Any two assignment methods mentioned in the 22OB2.4, if an assignment is project based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
4. The final CIE marks of the course out of 50 will be the sum of the scale down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester End Examination:**

Theory SEE will be conducted by the University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Text Book:**

1. W.H. Hayt and J.A. Buck, ―Engineering Electromagnetics, 8th Edition, Tata McGraw- Hill, 2014, ISBN-978-93-392-0327-6.

**Reference Books:**

1. Elements of Electromagnetics – Matthew N.O., Sadiku, Oxford University press, 4thEdn.
2. Electromagnetic Waves and Radiating systems – E. C. Jordan and K.G. Balman, PHI, 2ndEdn.
3. Electromagnetics- Joseph Edminister, Schaum Outline Series, McGraw Hill.
4. N. Narayana Rao, ―Fundamentals of Electromagnetics for Engineering, Pearson

**Web links and Video Lectures (e-Resources):**

- NPTEL Video lectures: https://youtu.be/pGdr9WLto4A
- NPTEL Video lectures: https://youtu.be/xn2IpxI991M

**ActivityBasedLearning(SuggestedActivitiesinClass)/Practical-Based Learning**

- Group Discussion/Quiz
- Demonstration of Electromagnetic concepts.
- Case Study on Medical Imaging devices.

| **-Course Outcomes** | **Pos** | | | | | | | | | | | | **PSOs** | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **a** | **B** | **c** | **d** | **E** | **f** | **g** | **h** | **i** | **J** | **k** | **l** | **m** | **n** | **O** |
| **CO1:**Develop a thorough understanding of different coordinate systems and Evaluate problems on electrostatic force and fields | 2 | 2 | 3 | 2 | 2 | - | - | - | - | - | - | 2 | 2 | - | - |
| **CO2:** Apply Gauss law to evaluate Electric fields due to different charge distributions and Volume Charge distribution by using Divergence Theorem. | 2 | 3 | 2 | 2 | 2 | 1 | - | - | - | - | - | 2 | 3 | - | - |
| **CO3:** Interpret the physical significance of Laplace's equation, Biot-Savart's law, Ampere's law, and Stokes' theorem for evaluating Magnetic field for different current configurations | 3 | 2 | 3 | 3 | 2 | 1 | - | - | - | - | - | 2 | 3 | - | - |
| **CO4:** Interpret magnetic force, potential energy and Magnetization with respect to magnetic materials and voltage induced in electric circuits. | 2 | 3 | 2 | 2 | 3 | 1 | - | - | - | - | - | 2 | 3 | - | - |
| **CO5:** Apply Maxwell's equations for time varying fields, EM waves in free space and conductors and Evaluate power associated with EM waves. | 3 | 3 | 3 | 3 | 3 | 1 | 3 | - | - | - | - | 2 | 2 | - | - |
| **Course Contribution to POs** | **2.4** | **2.6** | **2.6** | **2.4** | **2.4** | **1** | **3** | - | - | - | - | **2** | **2.6** | - | - |

| PRINCIPLES OF COMMUNICATION SYSTEMS | | Semester | 4 |
|---|---|---|---|
| Course Code | **22UEC411C** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 3:0:2:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory + 8-10 Lab slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |
| Examination nature (SEE) | Theory/practical | | |

**Course objectives:**

This course will enable students to

- Understand and analyze concepts of Analog Modulation schemes viz; AM, FM
- Design and analyze the electronic circuits for AM and FM modulation and demodulation.
- Understand the concepts of random variable and random process to model communication systems.
- Understand and analyze the concepts of digitization of signals.
- Evolve the concept of SNR in the presence of channel induced noise

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**MODULE-1**

**Random Variables and Processes:** Introduction, Probability, Conditional Probability, Random variables. Statistical Averages: Function of a random variable, Moments, Random Processes, Mean, Correlation and Covariance function: Properties of autocorrelation function, Cross–correlation functions, Gaussian Process: Gaussian Distribution Function. **[Text 2: 5.1, 5.2, 5.3, 5.4, 5.5, 5.6, 5.9]**

| MODULE-2 |
|---|
| **Amplitude Modulation Fundamentals:** AM Concepts, Modulation index and Percentage of Modulation, Sidebands and the frequency domain, AM Power, Single Sideband Modulation.<br>**AM Circuits:** Amplitude Modulators: Diode Modulator, Transistor Modulator, collector Modulator. AmplitudeDemodulators: Diode Detector, Balanced Modulators: Lattice Modulators.<br>**Frequency Division Multiplexing:** Transmitter-Multiplexer, Receiver-DE multiplexer.<br>**[Text1: 3.1, 3.2, 3.3, 3.4, 3.5, 4.2, 4.3, 4.4, 10.2]** |
| **MODULE-3** |
| **Fundamentals of Frequency Modulation:** Basic Principles of Frequency Modulation, Principles of Phase Modulation, Modulation index and sidebands, Noise Suppression Effects of FM, Frequency Modulation versus Amplitude Modulation.<br>**FM Circuits:** Frequency Modulators: Voltage Controlled Oscillators., Frequency Demodulators: Slope Detectors, Phase Locked Loops.<br>**Communication Receiver:** Super heterodyne receiver, Frequency Conversion: Mixing Principles, JFET Mixer. **[Text1: 5.1, 5.2, 5.3, 5.4, 5.5, 6.1, 6.3, 9.2, 9.3]** |
| **MODULE-4** |
| **Digital Representation of Analog Signals:** Introduction, Why Digitize Analog Sources? The Sampling process, Pulse Amplitude Modulation, Time-Division Multiplexing, Pulse Position Modulation: Generation and Detection of PPM wave. The Quantization Process. Pulse Code Modulation: Sampling, Quantization, Encoding, line Codes, Differential encoding, Regeneration, Decoding, filtering, multiplexing. **[Text2: 7.1, 7.2, 7.3, 7.4, 7.5, 7.6, 7.8, 7.9]** |
| **MODULE-5** |
| **Baseband Transmission of Digital signals:** Introduction, Inter symbol Interference, Eye Pattern, Nyquistcriterion for distortion less Transmission, Baseband M-array PAM Transmission.<br>**[Text2: 8.1, 8.4, 8.5, 8.6, 8.7]**<br>**Noise:** Signal to Noise Ratio, External Noise, Internal Noise, Semiconductor Noise, Expressing Noise Levels, Noisein Cascade Stages. **[Text1:9.5]** |

**PRACTICAL COMPONENT OF IPCC** *(Experiments can be conducted using MATLAB/SCILAB/OCTAVE)*

| Sl. NO. | Experiments |
|---|---|
| 1 | Basic Signals and Signal Graphing: a) unit Step, b) Rectangular, c) standard triangle d) sinusoidal and e) Exponential signal. |
| 2 | Illustration of signal representation in time and frequency domains for a rectangular pulse. |
| 3 | Amplitude Modulation and demodulation: Generation and display the relevant signals and its spectrums. |
| 4 | Frequency Modulation and demodulation: Generation and display the relevant signals and its spectrums. |
| 5 | Sampling and reconstruction of low pass signals. Display the signals and its spectrum. |
| 6 | Time Division Multiplexing and DE multiplexing. |

| | |
|---|---|
| 7 | PCM Illustration: Sampling, Quantization and Encoding |
| 8 | Generate a) NRZ, RZ and Raised cosine pulse, b) Generate and plot eye diagram |
| 9 | Generate the Probability density function of Gaussian distribution function. |
| 10 | Display the signal and its spectrum of an audio signal. |

**Course outcomes (Course Skill Set):**

At the end of the course, the student will be able to:

1. Understand the principles of analog communication systems and noise modelling.
2. Identify the schemes for analog modulation and demodulation and compare their performance.
3. Design of PCM systems through the processes sampling, quantization and encoding.
4. Describe the ideal condition, practical considerations of the signal representation for baseband transmission of digital signals.
5. Identify and associate the random variables and random process in Communication system design.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory componentare **25 marks** and that for the practical component is **25 marks**.

**CIE for the theory component of the IPCC**

1. 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
2. Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
3. The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

**CIE for the practical component of the IPCC**

1. **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
2. On completion of every experiment/program in the laboratory, the students shall be evaluated including viva- voce and marks shall be awarded on the same day.
3. The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write- ups are added and scaled down to **15 marks**.
4. The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
5. Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
6. The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component**.

a. The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
b. SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
c. The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken
d. together.

**Suggested Learning Resources**:

**Books**


1. Louis E Frenzel, Principles of Electronic Communication Systems, 3rd Edition, Mc Graw Hill Education(India) Private Limited, 2016. ISBN: 978-0-07-066755-6.
2. Simon Haykin & Michael Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN:978-81-265-2151-7.


**Reference Books**


1. B P Lathi, Zhi Ding, "Modern Digital and Analog Communication Systems", Oxford University Press., 4th edition, 2010, ISBN: 97801980738002.
2. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication systems", 4th Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-1-25-902985-1


**Web links and Video Lectures (e-Resources):**

1. Principles of Communication Systems **https://nptel.ac.in/courses/108104091**
2. Communication Engineering **https://nptel.ac.in/courses/117102059**

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

1. Assignments and test – Knowledge level, Understand Level and Apply level
2. Experiential Learning by using free and open source software's SCILAB or OCTAVE
3. Open ended questions by faculty, Open ended questions from students

| Control Systems | | | |
|---|---|---|---|
| Course Code | **22UEC412C** | CIE Marks | 50 |
| Teaching Hours/Week (L: T: P) | (3:0:2) | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours Theory + 12 Lab slots | Total Marks | 100 |
| Credits | 04 | Exam Hours | 03 |

**Course objectives: This course will enable students to:**

1. Understand basics of control systems and design mathematical models using block diagramreduction, SFG, etc.
2. Understand Time domain and Frequency domain analysis.
3. Analyze the stability of a system from the transfer function
4. Familiarize with the State Space Model of the system.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type ofteaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Linear Algebra & SignalProcessing.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotescritical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather thansimply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come upwith their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, ithelps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
10. Give Programming Assignments.

**Module-1**

**Introduction to Control Systems:** Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems -Mechanical Systems, Electrical Systems, Analogous Systems. (Textbook 1: Chapter 1.1, 2.2)

| Module-2 |
|---|
| **Block diagrams and signal flow graphs:** Transfer functions, Block diagram algebra and Signal Flow graphs. (Textbook 1: Chapter 2.4, 2.5, 2.6) |
| **Module-3** |
| **Time Response of feedback control systems:** Standard test signals, Unit step response of First and Second Order Systems. Time response specifications, Time response specifications of second order systems, steady state errors and error constants. Introduction to PI, PD and PID Controllers (excluding design). (Textbook 1: Chapter 5.3, 5.4, 5.5) |
| **Module-4** |
| **Stability analysis:** Concepts of stability, Necessary conditions for Stability, Routh stability criterion, Relative stability analysis: more on the Routh stability criterion.<br>**Introduction to Root-Locus Techniques**, The root locus concepts, Construction of root loci. (Textbook 1: Chapter 6.1, 6.2, 6.4, 6.5, 7.1, 7.2, 7.3) |
| **Module-5** |
| **Frequency domain analysis and stability:** Correlation between time and frequency response, Bode Plots, Experimental determination of transfer function. (Textbook 1: Chapter 4: 8.1, 8.2, 8.4) Mathematical preliminaries, Nyquist Stability criterion, (Stability criteria related to polar plots are excluded) (Textbook 1: 9.2, 9.3)<br>**State Variable Analysis:** Introduction to state variable analysis: Concepts of state, state variable and state models. State model for Linear continuous –Time systems, solution of state equations. (Textbook 1: 12.2, 12.3, 12.6) |

**PRACTICAL COMPONENT OF IPCC**

Using suitable simulation software (P-Spice/ MATLAB / Python / Scilab / OCTAVE / LabVIEW) demonstrate the operation of the following circuits:

| Sl. No. | Experiments |
|---|---|
| 1 | Implement Block diagram reduction technique to obtain transfer function a control system. |
| 2 | Implement Signal Flow graph to obtain transfer function a control system. |
| 3 | Simulation of poles and zeros of a transfer function. |
| 4 | Implement time response specification of a second order Under damped System, for different damping factors. |
| 5 | Implement frequency response of a second order System. |
| 6 | Implement frequency response of a lead lag compensator. |
| 7 | Analyze the stability of the given system using Routh stability criterion. |
| 8 | Analyze the stability of the given system using Root locus. |
| 9 | Analyze the stability of the given system using Bode plots. |
| 10 | Analyze the stability of the given system using Nyquist plot. |
| 11 | Obtain the time response from state model of a system. |
| 12 | Implement PI and PD Controllers. |
| 13 | Implement a PID Controller and hence realize an Error Detector. |
| 14 | Demonstrate the effect of PI, PD and PID controller on the system response. |

**Course Outcomes**

At the end of the course the student will be able to:

1. Deduce transfer function of a given physical system, from differential equation representation or Block Diagram representation and SFG representation.
2. Calculate time response specifications and analyze the stability of the system.
3. Draw and analyze the effect of gain on system behavior using root loci.
4. Perform frequency response Analysis and find the stability of the system.
5. Represent State model of the system and find the time response of the system.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam(SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together

**CIE for the theory component of IPCC**

Two Tests each of **20 Marks (duration 01 hour**)

- First test at the end of 5$^{th}$ week of the semester
- Second test at the end of the 10$^{th}$ week of the semester

Two assignments each of **10 Marks**

- First assignment at the end of 4$^{th}$ week of the semester
- Second assignment at the end of 9$^{th}$ week of the semester

Scaled-down marks of two tests and two assignments added will be CIE marks for the theory component of IPCC for **30 marks**.

**CIE for the practical component of IPCC**

- On completion of every experiment/program in the laboratory, the students shall be evaluated and marks shall be awarded on the same day. The **15 marks** are for conducting the experiment and preparation of the laboratory record, the other **05 marks shall be for the test** conducted at the end of the semester.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to 15 marks.
- The laboratory test **(duration 03 hours)** at the end of the 15$^{th}$ week of the semester /after completion of all the experiments (whichever is early) shall be conducted for 50 marks and scaled down to 05 marks**.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **20 marks**.

**SEE for IPCC**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (duration 03 hours)

- The question paper will have ten questions. Each question is set for 20 marks.
- There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under thatmodule.
- The students have to answer 5 full questions, selecting one full question from eachmodule.

**The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper shall include questions from the practical component**.

- The minimum marks to be secured in CIE to appear for SEE shall be the 12 (40% of maximum marks-30) in the theory component and 08 (40% of maximum marks -20) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 questions to be set from the practical component of IPCC, the total marks of all questions should not be more than the 20 marks.

SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify in the SEE. Marks secured out of 100 shall be reduced proportionally to 50.

**Suggested Learning Resources:**

**Text Books**

1. Control Systems Engineering, I J Nagrath, M. Gopal, New age international Publishers, Fifthedition.

**Web links and Video Lectures (e-Resources):**

- https://nptel.ac.in/courses/108106098

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

*Programming Assignments / Mini Projects can be given to improve programming skills*

| Communication Laboratory | | Semester | 4 |
|---|---|---|---|
| Course Code | **22UEC413C** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P: S) | 0:0:2 | SEE Marks | 50 |
| Credits | 01 | Exam Hours | 03 |
| Examination type (SEE) | Practical | | |

**Course objectives:**

This laboratory course enables students to

1. Understand the basic concepts of AM and FM modulation and demodulation.
2. Design and analyze the electronic circuits used for AM and FM modulation and demodulation circuits.
3. Understand the sampling theory and design circuits which enable sampling and reconstruction of analog signals.
4. Design electronic circuits to perform pulse amplitude modulation, pulse position modulation and pulse width modulation.

| | **Experiments** (Experiments to be conducted using hardware components) |
|---|---|
| 1 | Design and test a high-level collector Modulator circuit and Demodulation the signal using diode detector. |
| 2 | Test the Balanced Modulator / Lattice Modulator (Diode ring) |
| 3 | Design a Frequency modulator using VCO and FM demodulator using PLL (Use IC566 and IC565). |
| 4 | Design and plot the frequency response of Pre-emphasis and De-emphasis Circuits |
| 5 | Design and test BJT/FET Mixer |
| 6 | Design and test Pulse sampling, flat top sampling and reconstruction |
| 7 | Design and test Pulse amplitude modulation and demodulation. |
| 8 | Generation and Detection of Pulse position Modulation |
| 9 | Generation and Detection of Pulse Width Modulation |
| 10 | PLL Frequency Synthesizer |
| 11 | Data formatting and Line Code Generation |
| 12 | PCM Multiplexer and DE multiplexer |

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

1. Illustrate the AM generation and detection using suitable electronic circuits.
2. Design of FM circuits for modulation, demodulation and noise suppression.
3. Design and test the sampling, Multiplexing and pulse modulation techniques using electronic hardware.
4. Design and Demonstrate the electronic circuits used for RF transmitters and receivers.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation (CIE):**

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

**Semester End Evaluation (SEE):**

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.

- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

**Suggested Learning Resources:**

1. Louis E Frenzel, Principles of Electronic Communication Systems, 3rd Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-0-07-066755-6.

| MICROCONTROLLERS | | Semester | 4 |
|---|---|---|---|
| Course Code | **22UEC414B** | CIE Marks | 50 |
| Teaching Hours/Week(L:T:P) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type(SEE) | Theory | | |

**Course objectives:**

This course will enable students to:

- Understand the difference between Microprocessor and Microcontroller and embedded microcontrollers.
- Analyze the basic architecture of 8051microcontroller.
- Program 8051 microcontroller using Assembly Language and C.
- Understand the operation and use of inbuilt Timers/Counters and Serial port of 8051
- Understand the interrupt structure of 8051 and Interfacing I/O devices using I/O ports of 8051.

**Teaching-Learning Process (General Instructions)**

The samples strategies, which the teacher can use to accelerate the attainment of the variouscourse outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but adifferent type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative(Group)Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical kills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the students' understanding.
   Give Programming Assignments.

**Module-1 ( 8 Hrs )**

**Microcontroller:** Microprocessor Vs Microcontroller, Micro controller & Embedded Processors, Processor Architectures-Harvard Vs Princeton & RISC Vs CISC, 8051 Architecture- Registers, Pin diagram, I/Oports functions, Internal Memory organization. External Memory (ROM & RAM) interfacing. (Text book 1-1.1,Text book 2-1.0,1.1,3.0,3.1,3.2,3.3 Textbook 3-Pg 5-9)

**Module-2 ( 8 Hrs )**

**Instruction Set:** 8051 Addressing Modes, Data Transfer Instructions, Arithmetic instructions, Logical Instructions, Jump & Call Instructions Stack & Subroutine Instructions of 8051 (with examples in assembly Language). (Text book 2- Chapter 5,6,7,8, **Additional reading Refer Textbook 3, Chapter 3 for complete understanding of instructions with flow diagrams)**

**Module-3 ( 8 Hrs )**

**Timers/Counters & Serial port programming**:
Basics of Timers & Counters, Data types & Time delay in the 8051 using C, Programming 8051 Timers, Mode 1 & Mode 2 Programming, Counter Programming (Assembly Language only). (Text book 2- 3.4, Text book 1- 7.1, 9.1,9.2)
Basics of Serial Communication, 8051 Connection to RS232, Programming the 8051 to transfer data serially & to receive data serially using C.( Text book 2- 3.5, Text book 1- 10.1,10.2,10.3 except assembly language programs, 10.5)

**Module-4 ( 8 Hrs )**

**Interrupt Programming:** Basics of Interrupts, 8051 Interrupts, Programming Timer Interrupts, Programming Serial Communication Interrupts, Interrupt Priority in 8051(Assembly Language only) ( Text book 2- 3.6, Text book 1- 11.1,11.2,11.4, 11.5)

**Module-5 ( 8 Hrs )**

**I/O Port Interfacing & Programming:** I/O Programming in 8051 C, LCD interfacing, DAC 0808 Interfacing, ADC 0804 interfacing, Stepper motor interfacing, DC motor control & Pulse Width Modulation (PWM) using C only. (Text book 1- 7.2, 12.1, 13.1, 13.2, 17.2, 17.3)

**Course outcome (Course Skill Set)**

At the end of the course, students will be able to:

1. Describe the difference between Microprocessor and Microcontroller, Types of Processor Architectures and Architecture of 8051Microcontroller.
2. Discuss the types of 8051 Microcontroller Addressing modes & Instructions with Assembly Language Programs.
3. Explain the programming operation of Timers/Counters and Serial port of 8051 Microcontroller.
4. Illustrate the Interrupt Structure of 8051 Microcontroller & its programming.
5. Develop C programs to interface I/O devices with 8051 Microcontroller.

.**Continuous Internal Evaluation:**

There are 25marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.

Each test shall be conducted for 25marks.The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks

1. Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the courses hall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
2. The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's**

**taxonomy as per the outcome defined for the course.Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common questionpapers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20marks.
2. There will be 2questions from each module. Each of the two questions under a module (with amaximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to50 marks

**Suggested Learning Resources:**

**TEXT BOOKS**

1. The "8051 Microcontroller and Embedded Systems – Using Assembly and C", Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollind. Mckinlay; Phi, 2006 / Pearson, 2006.
2. "The 8051 Microcontroller", Kenneth j. Ayala, 3rd edition, Thomson/Cengage Learning.
3. "Programming And Customizing The 8051 Microcontroller".,Myke Predko Tata Mc Graw-Hill Edition 1999 (reprint 2003).

**REFERENCEBOOKS:**

1. "The 8051 Microcontroller Based Embedded Systems", Manish K Patel, McGraw Hill, 2014, ISBN: 978-93-329-0125-4.

"Microcontrollers: Architecture, Programming, Interfacing and System Design", Raj Kamal, Pearson Education, 2005.

**Web links and Video Lectures(e-Resources):**

**https://youtu.be/pA6K5NgWTow?si=zQqqgXQq50dVL_-s**

| Industrial Electronics | | Semester | IV |
|---|---|---|---|
| Course Code | **22UEC414C** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 hours | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |
| Examination type (SEE) | Theory | | |

**Course objectives:** This course will enable student to

- Explain broad types of industrial power devices, there structure, and its characteristics.
- Design and analyze the broad categories of power electronic circuits.
- Explain various types of MEMs devices, principle of operation and construction.
- Familiarize with soft core processors and computer architecture.
- Apply protective methods for devices and circuits.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**Module-1**

**Industrial Power Devices:** General purpose power diodes, fast recovery power diodes, schottky power diodes, silicon carbide power diodes **(Text book 1: 2.5, 2.6)**, Power MOSFETs, Steady state characteristics, switching characteristics, silicon carbide MOSFETs, COOLMOS, Junction field effect transistors, operation and characteristics of JFETs, Silicon Carbide JFET structures, Bipolar Junction Transistors, Steady state characteristics, switching characteristics, silicon carbide BJTs, IGBT, silicon carbide IGBTs

**(Text book 1: 4.3, 4.4, 4.6, 4.7**

**Module-2**

**Power Electronics Circuits:)**, Thyristor, Thyristor characteristics, two transistor model **(Text book 1: 9.2, 9.3, 9.4)**. Controlled Rectifiers – Single phase full converter with R and RL load, Single phase dual converters, and Three phase full converter with RL load **(Text book 1: 10.2,**

**10.3, 10.4)**. Switching mode regulators – Buck Regulator, Boost regulator, Buck – Boost regulator, comparison of regulators.

**(Text book 1: 5.9.1, 5.9.2, 5.9.3, 5.10)**

**Module-3**

**Inverters** – Principle of operation, Single phase bridge inverter, Three phase inverter with 180 and 120 degree conduction, Current source inverter **(Text book 1: 6.3, 6.4, 6.5, 6.9)**.

**AC voltage controllers** – Single phase full wave controller with resistive load, single phase full wave controller with inductive load **(Text book 1: 11.3, 11.4)**.

**Module-4**

**MEMS Devices:** Sensing and Measuring Principles, Capacitive Sensing, Resistive Sensing, Piezoelectric Sensing, Thermal Transducers, Optical Sensors, Magnetic Sensors, MEMS Actuation Principles, Electrostatic Actuation, Thermal Actuation, Piezoelectric Actuation, Magnetic Actuation, MEMS Devices Inertial Sensors, Pressure Sensors, Radio Frequency MEMS: Capacitive Switches and Phase Shifters, Microfluidic Components, Optical Devices. **(Text book 2: 13.1, 13.3, 13.4)**

**MEMS Applications:** Introduction, Industrial, Automotive, Biomedical.

(**Text book 2:15.1, 15.2, 15.3, 15.4)**

**Module-5**

**Protections of Devices and Circuits:** Cooling and Heat sinks, Thermal Modeling of Power Switching Devices, Electrical Equivalent Thermal model, Mathematical Thermal Equivalent Circuit, Coupling of Electrical and Thermal Components, Snubber circuits, Voltage protection by Selenium Diodes and Metal oxide Varistors, Current protection, Fusing, Fault current with AC source, Fault current with DC source, Electromagnetic Interference, sources of EMI, Minimizing EMI Generation, EMI shielding, EMI standards.

**(Text book 1: 17.2, 17.3, 17.4, 17.5, 17.6, 17.7, 17.8, 17.9)**.

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to:

1. Explain different types of industrial power devices such as MOSFET, BJT, IGBT etc, therestructure, and its operating characteristics.
2. Design and analyze the power electronic circuits such as switch mode regulators, inverters,controlled rectifiers and ac voltage controllers.
3. Explain various types of MEMs devices used for sensing pressure, temperature, current,voltage, humidity, vibration etc...
4. Familiarize with soft core processors such as ASIC and FPGA.
5. Familiarize with computer hardware, software, architecture, instruction set, memory organization, multiprocessor architecture.
6. Apply protective methods for devices various industrial power devices based on thermal requirements and develop protective methods for the circuits against various electrical parameters.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based thenonly one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests andassignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomyas per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers forthe course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximumof 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

**Suggested Learning Resources:**

**Text Books**

1. Power Electronics: Devices, Circuits, and Applications, Muhammad H. Rashid, Pearson, 4th International edition.
2. Fundamentals of Industrial Electronics, Bogdan M. Wilamowski, J. David Irwin, CRC Press, 2011,

**Reference Books**

1. Thomas E. Kissell, Industrial Electronics: Applications for Programmable Controllers, Instrumentation and Process Control, and Electrical Machines and Motor Controls, 3rd edition, 2003, Prentice Hall.
2. Ned Mohan, T.M. Undeland and W.P. Robbins, "Power Electronics: Converters, Applications and Design", Wiley India Ltd, 2008.

**Web links and Video Lectures (e-Resources):**

- https://archive.nptel.ac.in/courses/108/102/108102145/
- https://nptel.ac.in/courses/117105082
- https://www.youtube.com/channel/UCKg8GNii0Q-ieXE56AXosGg/featured
- https://www.ieee-ies.org/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

- Quiz and Seminars

| OPERATING SYSTEM | | Semester | 4 |
|---|---|---|---|
| Course Code | **22UEC414D** | CIE Marks | 50 |
| Teaching Hours/Week(L:T:P) | 3:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 3 |
| Examination type(SEE) | Theory | | |

**Course objectives:**

This course will enable students to:

- Understand the services provided by an operating system.
- Explain how processes are synchronized and scheduled.
- Understand different approaches of memory management and virtual memory management. Describe the structure and organization of the file system
- Understand inter-process communication and deadlock situations.

**Teaching-Learning Process (General Instructions)**

The samples strategies, which the teacher can use to accelerate the attainment of the variouscourse outcomes are listed in the following:

**1.** Lecturer method (L) need not to be only traditional lecture method, but alternative effective teaching methods could be adopted to attain the outcomes.
**2.** Use of Video/Animation to explain functioning of various concepts.
**3.** Encourage collaborative (Group Learning) Learning in the class.
**4.** Ask at least three HOT (Higher order Thinking) questions in the class, which promotes critical thinking.
**5.** Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop design thinking skills such as the ability to design, evaluate, generalize, and analyze information rather than simply recall it.
**6.** Introduce Topics in manifold representations.
**7.** Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
**8.** Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**Module-1**

**Introduction to Operating Systems:** OS, Goals of an OS, Operation of an OS,Computational Structures, Resource allocation techniques, Efficiency, System Performance and User Convenience, Classes operating System, Batch processing, Multi programming, Time Sharing Systems, Real Time and distributed Operating Systems **(Topics from Sections 1.2, 1.3, 2.2 to 2.8 of Text).**

**Module-2**

| |
|---|
| **Process Management:** OS View of Processes, PCB, Fundamental State Transitions of aprocess, Threads, Kernel and User level Threads, Non-preemptive scheduling- FCFS andSRN, Preemptive Scheduling- RR and LCN, Scheduling in Unix and Scheduling in Linux**(Topics from Sections 3.3, 3.3.1 to 3.3.4, 3.4, 3.4.1, 3.4.2, Selected scheduling topics from 4.2 and 4.3 , 4.6, 4.7 of Text).** |
| **Module-3** |
| **Memory Management:** Contiguous Memory allocation, Non-Contiguous Memory Allocation, Paging, Segmentation, Segmentation with paging, Virtual Memory Management, Demand Paging, VM handler, FIFO, LRU page replacement policies, Virtual memory in Unix and Linux. **(Topics from Sections 5.5 to 5.9, 6.1 to 6.3 except Optimal policy and 6.3.1, 6.7,6.8 of Text)** |
| **Module-4** |
| **File Systems:** File systems and IOCS, File Operations, File Organizations, Directory structures, File Protection, Interface between File system and IOCS, Allocation of disk space, Implementing file access. **(Topics from Sections 7.1 to 7.8 of Text).** |
| **Module5** |
| **Message Passing and Deadlocks:** Overview of Message Passing, implementing message passing, Mailboxes, Deadlocks, Deadlocks in resource allocation, Handling deadlocks, Deadlock detection algorithm, Deadlock Prevention **(Topics from Sections 10.1 to 10.3, 11.1 to 11.5 of Text).** |

**Course outcome (Course Skill Set)**

At the end of the course, students will be able to:

1. Explain the goals, structure, operation and types of operating systems.
2. Apply scheduling techniques to find performance factors.
3. Explain organization of file systems and IOCS.
4. Apply suitable techniques for contiguous and non-contiguous memory allocation.
5. Describe message passing, deadlock detection and prevention methods.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE)is 50%.The minimum passing mark for the CIE is 40%of the maximum marks(20marks out of 50) and forthe SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

There are 25marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.

Each test shall be conducted for 25marks.The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of thesyllabus. The average of the two tests shall be scaled down to 25 marks

Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the courses hall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks) The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests andassignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Blo om's taxonomy as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20marks.
2. There will be 2questions from each module. Each of the two questions under a module (with amaximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Marks scored shall be proportionally reduced to50 marks

**Suggested Learning Resources:**

**TEXT BOOKS**

| Data Structures Using C | | Semester | IV |
|---|---|---|---|
| Course Code | **22UEC414A** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | 3:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 40 | Total Marks | 100 |
| Credits | 03 | Exam Hours | 03 |
| Examination nature (SEE) | Theory | | |

**COURSE OVERVIEW:**

**COURSE OBJECTIVES:**

The objectives of this course are to:

1. Develop proficiency in designing and implementing fundamental data structures.
2. Learn various sorting and searching algorithms and analyze their time complexity.
3. Understand algorithmic problem-solving techniques, including recursion.
4. Explore advanced data structures like trees, graphs, and hash tables.
5. Apply data structures and algorithms knowledge to solve real-world programming challengesefficiently.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. The lecturer's approach (L) does not have to be limited to traditional methods of teaching. It is possible to incorporate alternative and effective teaching methods to achieve the desired outcomes.
2. Utilize videos and animations to illustrate the functioning of different techniques used in themanufacturing of smart materials.
3. Foster collaborative learning exercises within the classroom to encourage group participationand engagement.
4. Pose a minimum of three Higher Order Thinking (HOT) questions during class discussions to stimulate critical thinking among students.
5. Implement Problem-Based Learning (PBL) as an approach that enhances students' analyticalskills and nurtures their ability to design, evaluate, generalize, and analyze information, rather than solely relying on rote memorization.

**Module-1**

Arrays:1D,2D and multidimensional.
Pointers: Definition and Concepts, Array of pointers, Structures and unions. Array of structures, pointer arrays, pointer to structures. Passing pointer variable as parameter in functions Dynamic memory allocation: malloc (), calloc (), realloc () and free function.Introduction to data structures and algorithms
Text book 1 -Chapter-1.1-1.3 except Rational Numbers.
Text Book 2, chapter-2

| **Module-2** |
| --- |
| The Stack – Definition and examples, primitive operations, Example. Representing Stacks in C, Example: Infix, Postfix and Prefix, converting an Expression from Infix to Prefix and Program.<br>Text Book -1-Chapter – 2.1-2.3<br>Recursion – Recursive Definition and Processes, Recursion in C, Writing Recursive<br>Programs.Recursions - Text Book -1-Chapter – 3.1-3.3 |
| **Module-3** |
| Queues and Lists – The Queue and its sequential representation, Linked Lists, Lists in C.<br>Other Lists structures – Circular Lists, Stacks, Queues as circular list. The Josephus problem, doublylinked lists.<br>Linked lists and Queues - Text Book -1-Chapter – 4.1-4.3, 4.5 |
| **Module-4** |
| Trees – Binary Trees, binary tree representations, Huffman algorithm, Trees and their applications.<br>Searching – Basic searching Techniques, Tree Searching.<br>Trees - Text Book -1-Chapter – 5.1-5.3, 5.5, 7.1, 7.2 |
| **Module-5** |
| Hashing – Introduction, Static Hashing, Dynamic HashingText Book 3<br>-8.1 – 8.3<br>Graphs - Graph representation, Elementary graph operations, Minimum cost spanning<br>Trees –Kruskal's Algorithm, Prim's algorithm Text Book 3 - 6.1, 6.2, 6.3.1, 6.3.2 |

**Course Outcomes (COs) (Course Skill Set)**

At the end of the course, the student will be able to:

1. Master the implementation and application of key data structures in programming.
2. Demonstrate the ability to analyze algorithm efficiency and optimize code.
3. Solve complex problems by applying algorithmic strategies and techniques.
4. Design and implement algorithms for tasks involving searching, sorting, and graph traversal.
5. Utilize data structures and algorithms to enhance software performance and scalability

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemedto have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- For the Assignment component of the CIE, there are 25 marks and for the Internal AssessmentTest component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and thesecond test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and othermethods of assessment.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.**

**Semester-End Examination (SEE):**

Theory SEE will be conducted by University as per the scheduled timetable, with common question

papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

**Suggested Learning Resources:**

TEXT BOOKS:

1. Data Structures using C and C++, Yedidyah, Augenstein, Tannenbaum, 2nd Edition, PearsonEducation, 2007.
2. Data Structures using C, Reema Thareja, 2nd Edition, Oxford University Press, 2011
3. Fundamentals of Data structures in C, 2nd Edition, Horowitz, Sahni, Anderson freedUniversities Press,2008

REFERENCEBOOKS:

1. Reema Thareja, Computer fundamentals and programming in C, second edition, OxfordUniversity Press.
2. Gilberg and Forouzan, Data Structures: A Pseudo-code approach with C, 2ndEd,CengageLearning,2014.

**Web links and Video Lectures (e-Resources):**

- https://archive.nptel.ac.in/courses/106/102/106102064/
- https://archive.nptel.ac.in/courses/106/106/106106127/
- https://nptel.ac.in/courses/106102064
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS35.html
- https://nptel.ac.in/courses/106/105/106105171/
- http://www.nptelvideos.in/2012/11/data-structures-and-algorithms.html
- http://elearning.vtu.ac.in/econtent/courses/video/CSE/06CS43.html
- https://nptel.ac.in/courses/106/101/106101060/

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning**

Real world problem solving using group discussion.

- Back/Forward stacks on browsers.
- Undo/Redo stacks in Excel or Word.
- Linked list representation of real-world queues -Music player, image viewer
- Real world problem solving and puzzles using group discussion. E.g., Fake coin identification, Peasant,wolf, goat, cabbage puzzle, Konigsberg bridge puzzle etc.,

Demonstration of solution to a problem through programming.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation(CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling thelaboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up willbeevaluatedfor10marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-upon time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted

| Microcontrollers Lab | | Semester | 4 |
|---|---|---|---|
| Course Code | **22UEC415D** | CIE Marks | 50 |
| Teaching Hours/Week(L:T:P) | 0:0:2 | SEE Marks | 50 |
| Credits | 01 | Total Marks | 100 |
| | | Exam Hours | 2 |
| Examination type(SEE) | Practical | | |

**Course objectives:** This course will enable students to:

- Understand the basic programming of Microcontrollers.
- Developthe8051 Microcontroller-based programs for various applications using Assembly Language & CProgramming.
- Program8051Microcontrollertocontrolanexternalhardwareusingsuitable I/Oports.

| | |
|---|---|
| **Note** | Execute the following experiments by using Keil Microvision Simulator (any 8051 Microcontroller can be chosen as the target) and Hardware Interfacing Programs using 8051 Trainer Kit. |
| **Sl.No** | **I. Assembly Language Programming** |
| **Data Transfer Programs:** | |
| 1 | Write an ALP to move a block of n bytes of data from source (20h) to destination (40h) usingInternal-RAM. |
| 2 | Write an ALP to move a block of n bytes of data from source (2000h) to destination (2050h) using External RAM. |
| 3 | Write an ALP to exchange the source block starting with address 20h, (Internal RAM) containing N (05) bytes of data with destination block starting with address 40h (Internal RAM). |
| 4 | Write an ALP to exchange the source block starting with address 10h (Internal memory), containingn (06) bytes of data with destination block starting at location 00h (External memory). |
| **Arithmetic & Logical Operation Programs:** | |
| 5 | Write an ALP to add the byte in the RAM at 34h and 35h, store the result in the register R5 (LSB)and R6 (MSB), using Indirect Addressing Mode. |
| 6 | Write an ALP to subtract the bytes in Internal RAM 34h &35h store the result in register R5 (LSB) & R6 (MSB). |
| 7 | Write an ALP to multiply two 8-bit numbers stored at 30h and 31h and store16- bit result in 32h and 33h of Internal RAM. |
| 8 | Write an ALP to perform division operation on 8-bit number by 8-bit number. |
| 9 | Write an ALP to separate positive and negative in a given array. |
| 10 | Write an ALP to separate even or odd elements in a given array. |
| 11 | Write an ALP to arrange the numbers in Ascending & Descending order. |

| | |
|---|---|
| 12 | Write an ALP to find Largest & Smallest number from a given array starting from 20h & store it in<br>Internal Memory location 40h. |
| **Counter Operation Programs:** | |
| 13 | Write an ALP for Decimal UP-Counter. |
| 14 | Write an ALP for Decimal DOWN-Counter. |
| 15 | Write an ALP for Hexadecimal UP-Counter. |
| 16 | Write an ALP for Hexadecimal DOWN-Counter. |
| **II. C Programming** | |
| 1 | Write an 8051 C program to find the sum of first 10 Integer Numbers. |
| 2 | Write an 8051 C program to find Factorial of a given number. |
| 3 | Write an 8051 C program to find the Square of a number (1 to 10) using Look-Up Table. |
| 4 | Write an 8051 C program to count the number of Ones and Zeros in two consecutive memory<br>locations. |
| **III. Hardware Interfacing Programs** | |
| 1 | Write an 8051 C Program to rotate stepper motor in Clock & Anti-Clockwise direction. |
| 2 | Write an 8051 C program to Generate Sine & Square waveforms using DAC interface. |

**Course outcomes (Course Skill Set):** At the end of the course the student will be able to:

1. Write a Assembly Language / C program using 8051for solving simple problems that manipulate input data using different instructions.
2. Develop Testing and experimental procedures on 8051 Microcontroller, Analyze their operationunder different cases.
3. Developprogramsfor8051Microcontrollertoimplementreal world problems.
4. DevelopMicrocontrollerapplicationsusingexternalhardwareinterface.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and forthe SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ courseif the student secures a minimum of40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation(CIE):**

CIEmarksforthepracticalcourseare**50Marks**.

The split-up of CIE marks for record/journalandtestareintheratio**60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up.Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10marks.
- Total marks scored by the students are scaled down to **30marks**(60%ofmaximummarks).
- Weightagetobegivenforneatnessandsubmissionofrecord/write-upontime.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write- up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20marks** (40%ofthemaximummarks). The Sum of scaled-down marks scored in the report write-up /journal and marks of a test is the total CIE marks scored by the student.

**Semester End Evaluation(SEE):**

- SEE marks for the practical courseare50Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva- voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15%ofMarksallottedtotheprocedurepartaretobemadezero.The minimum duration of SEE is 02 hours

**Suggested Learning Resources:**

"The 8051 Microcontroller: Hardware, Software and Applications", V Udayashankara and M S Mallikarjuna Swamy, McGraw Hill Education,1st edition,2017.

| PROGRAMMABLE LOGIC CONTROLLER (PLC) | | Semester | IV |
|---|---|---|---|
| Course Code | **22UEC415B** | CIE Marks | 50 |
| Teaching Hours/Week (L: T:P: S) | 1:0:0:0 | SEE Marks | 50 |
| Total Hours of Pedagogy | 14 to 16 hours | Total Marks | 100 |
| Credits | 01 | Exam Hours | 01 |
| Examination type (SEE) | Theory | | |

**Course objectives:** This course will enable student to

- To understand the need for automation in the industry with basic controller mechanisms involved.
- To study programming concepts to achieve the desired goal or to define the various steps involved in the automation.
- To understand programming involved with basic subroutine functions.
- To make use of the internal hardware circuits of automation circuit to control the devices during various states by monitoring the timers and counters.
- To handle the data of the I/O devices to interface the data with the controller and auxiliary devices.

**Teaching-Learning Process (General Instructions)**

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking.
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

**Module-1**

**Introduction**: Programmable logic controller (PLC), role in automation (SCADA), advantages and disadvantages, hardware, internal architecture, sourcing and sinking **(Textbook 1: 1.1 to 1.4)**

**I/O devices and Processing:** list of input and output devices, examples of applications. I/O processing, input/output units, signal conditioning, remote connections, networks, processing inputs I/O addresses.

**(TextBook1: 2.1 to 2.3 and 4.1 to 4.7).**

**Module-2**

**Programming**: Ladder programming- ladder diagrams, logic functions, latching, multiple outputs, entering programs, functional blocks, program examples like location of stop and emergency switches. (**TextBook1: 5.1 to 5.7).**

**Module-3**

**Programming Methods:** Instruction Lists- Ladder programs and Instruction lists, Branch codes, Programming Examples- Signal lamp-valve operation task. Sequential Function Charts- Branching and convergence. **(TextBook1: 6.1 to 6.3).**

**Module-4**

**Internal Relays:** ladder programs, battery-backed relays, one-shot operation, set and reset, master control relay (**TextBook1: 7.1 to 7.6).**

**Timers and counters:** Types of timers, ON and OFF- delay timers, pulse timers, forms of counter, programming, up and down counters. **(TexBook1: 9.1 to 9.6).**

**Module-5**

**Shift register and data handling**: shift registers, ladder programs, registers and bits, data handling, arithmetic functions. **(TextBook1: 11.1 to 11.2 and 12.1 to 12.3)**

**Course outcome (Course Skill Set)**

At the end of the course, the student will be able to:

1. Describe the PLC and how to construct PLC ladder diagrams.
2. Illustrate an application with programming.
3. Describe characteristics of registers and conversion examples.
4. Apply PLC functions to timing and counting applications.
5. Analyze the analog operation of PLC and demonstrate the robot applications with PLC.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

**Continuous Internal Evaluation:**

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned.
- The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the

sum of the two assignments shall be scaled down to 25 marks)

- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests andassignment/s marks.

**Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy**
**as per the outcome defined for the course.**

**Semester-End Examination:**

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers forthe course (**duration 01 hours).**

1. SEE paper shall be set for 50 questions, each of the 01 marks. The pattern of the question paper is MCQ (multiple choice questions).
2. The time allotted for SEE is 01 hour. The student has to secure a minimum of 35% of the maximummarks meant for SEE.

**Suggested Learning Resources:**

**Textbooks:**

1. Programmable Logic Controllers-W Bolton, 5th edition/6th edition, Elsevier- newness, 2009/2015.
2. Programmable logic controllers - principles and applications"-John W. Webb, Ronald A Reiss, Pearsoneducation, 5th edition, 2007.

**Reference Books:**

1 Programmable Logic Controllers"- E. A Paar, 3rd Edition, An Engineers Guide. Newness, 2003.

2 "Introduction to Programmable Logic Controller"- Garry Dunning, 3rd Edition, Thomson Asia Pte Ltd.Publication, 2006

3 "PLCs & SCADA - Theory and Practice"- Rajesh Mehra, Vikrant Vij, 2nd Edition, Laxmi publication, 2017

4 "PLC Programming for Industrial Automation"- Kevin Collins, 1st Edition, Kindle, 2016

**Activity Based Learning (Suggested Activities in Class)/ Practical Based learning.**

- Quiz and Seminars

| Octave Programming | | | |
|---|---|---|---|
| Course Code | **22UEC415A** | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P:S) | 0:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | 12 Sessions | Total | 100 |
| Credits | 01 | Exam Hours | 02 |

**Additional One hour may be considered for instructions ifrequired*

Course objectives:

- Apply theoretical knowledge of Octave programming to practical programming tasks.
- Gain hands-on experience in implementing and debugging octave Programming through codingexercises and projects.

Course Syllabus: Basic data structures in Octave – Vectors, Matrices, Cell Arrays. Special vecors. Linear sampling and logarithmic sampling. Accessing elements of vectors, matrices, and matrices. Mathematical operations on vectors and matrices. Addition, Multiplication, Subtraction, Division, Power, Square-Root, trigonometric operations. Dot Products and Cross Products of Vectors. Matrix multiplication, matrix inverse and matrixtranspose operations. Finding eigen values and vectors of a square matrix. Finding the solution of a system of linear equations. Linear programming and integer linear programming using glpk. Plotting in Octave. Subplots, Stem Plots, Semilog and Log-log plots. Packages in Matlab – symbolic, signal processing, control. Applications of Octave to solve problems in Electrical engineering, Electronics engineering,Control Systems, Signals and Systems/Signal Processing.

| Sl..NO | Experiments |
|---|---|
| 1 | (a) Define the following matrices using Octave<br>i. A 4x4 identity matrix<br>ii. A 4x4 matrix of zeros<br>iii. A 4x4 matrix of ones<br>iv. The matrix U4 defined below.<br>$\begin{matrix}1 & 2 & 3 & 4\\ 2 & 3 & 1 & 4\\ 1 & 3 & 2 & 4\\ 4 & 3 & 1 & 2\end{matrix}$<br>v. Matrix D4 defined below. It is also called the Hadamard matrix of dimension 4.<br>$\begin{matrix}1 & 1 & 1 & 1\\ 1 & -1 & 1 & -1\\ 1 & 1 & -1 & -1\\ 1 & -1 & -1 & 1\end{matrix}$<br>vi. Matrix H4 defined below<br>$\mathbf{H}_4 = \frac{1}{\sqrt{4}}\begin{bmatrix}1 & 1 & 1 & 1\\ 1 & 1 & -1 & -1\\ \sqrt{2} & -\sqrt{2} & 0 & 0\\ 0 & 0 & \sqrt{2} & -\sqrt{2}\end{bmatrix}$<br>vii. A 4x4 magic square G4<br>viii. A 4x4 matrix of random numbers selected from the range {-1,0,1}.<br>ix. A 4x4 matrix of random numbers in the range 0 to 1.<br>(b)<br>(i) How can you generate a 4x4 matrix of all 2's?<br>(ii) Find the transpose of U4.<br>(iii) Multiply D4 by its transpose and obtain the resulting matrix. How is |

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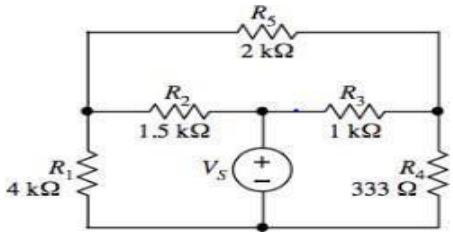
| | related to the identify matrix?<br>(iv) Find the inverse of H4 and verify that it is the inverse.<br>(v) What is the determinant of D4?<br>(vi) Extract the diagonal elements of H4.<br>(vii) How can you reshape the elements of D4 into a 2x8 matrix?<br>(viii) What is the magic sum of a 4x4 matrix? How can you verify that G4 is indeed a magic square?<br>(ix) The matrix D4 mentioned above is a 4x4 matrix. We wish to extract the sub- matrix consisting of rows 1 and 4 and columns 1 and 4. [In other words, the four corners of D4.) Show Octave code for generating the submatrix SM.<br>(x) Check if the H4 and D4 are orthogonal matrices. |
| 2 | You will have learnt Kirchhoff's current and voltage laws to solve the voltages and currents in a DC circuit. Given a circuit with n loops, we can write down n equations in n unknowns (loop currents). Alternately, given a circuit with n nodes, we can write down n equations in n unknowns (node voltages). These linear equations can be solved using Octave.<br><br>(a) Write down the KCL and KVL for the following circuit and solve the node voltages and currents. Assume that Vs is 100V.<br><br>  <br><br><br>(b) Find the total power dissipated in the circuit.<br>(c) Find the total power supplied by the voltage source.<br>(d) Challenge – Instead of hardcoding the values of the resistors and the voltage source, can you allow the user to input R1, R2, R3, R4, R5, and Vs? Develop a complete Octave script which reads in the values of circuit parameters and prints the node voltages, node currents, and power dissipation.<br>(e) Variations of the above exercises can be given to the students. For example, a resistor can be included in series with Vs. Alternately, a different circuit from a text book can be given. You can also change the problem by specifying the current through one of the resistors and asking the user to solve for Vs. |

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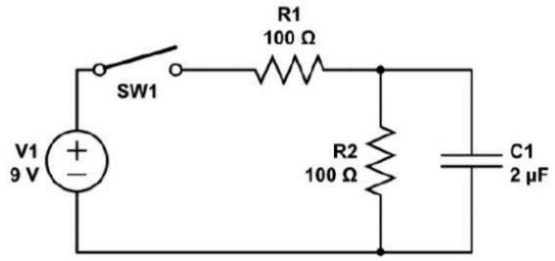
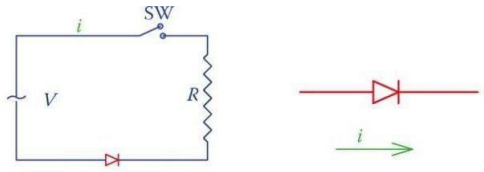
| 3 | (a) Consider the RC circuit shown in the figure below. Plot the voltage across C and the charging current through C when the switch is turned on.<br>(b) What is the rise time of the capacitor voltage? |
| |  |
| 4 |  <br>(a) The figure shows a diode-based rectifier. The diode conducts only when the input voltage is positive. Assume that it is an ideal diode. Plot the half-wave rectified waveform if the input to the rectifier is a 50-Hz sine wave of 200V RMS. Plot the output waveform for four cycles of the input.<br>(b) Find the average of the Half wave-rectified output in Octave and verify your answerusing the formula for the average output.<br>(c) Plot the output of a full-wave rectifier.<br>(d) Find the RMS value of the Full wave-rectified output in Octave and verify youranswer using the formulafor the RMS value.<br>(e) Assume that the input voltage is 2sin(500t) V and that the diode has a cut-in voltage of 0.6V. Plot thehalf-wave and full-wave rectified waveforms and find their average and RMS values. |
| 5 | (a) Given Z parameters, obtain the Y parameters using a function called Z2Y () Given Y parameters, obtain the Z parameters using afunction called Y2Z ()<br>(b) Find the Z and Y parameters for the T-network |

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| | **Assessment Details (both CIE and SEE)**<br>The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to havesatisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).<br>**Continuous Internal Evaluation(CIE):**<br>CIE marks for the practical course is **50 Marks**.<br>The split-up of CIE marks for record/journal and test are in the ratio **60:40**.<br>• Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of the practical session.<br>Record should contain all the specified experiments in the syllabus and each experiment write-up willbeevaluatedfor10marks.<br>• Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).<br>• Weightage to be given for neatness and submission of record/write-upon time.<br>• Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the $8^{th}$<br>week of the semester and these test shall be conducted after the $14^{th}$week of the semester.<br>• In each test, write-up, conduction of experiment, acceptable result, and procedural knowledge willcarry a weightage of 60% and the rest 40% for viva-voce.<br>• The suitable rubrics can be designed to evaluate each student's performance and learning ability.<br>Rubrics suggested in Annexure-II of Regulation book<br>• The average of 02 tests is scaled down to **20 marks** (40%of the maximum marks).<br>• The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the totalCIE marks scored by the student. |
| | **Semester End Evaluation(SEE):**<br>SEE marks for the practical course is 50Marks.<br>SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by theUniversity All laboratory experiments are to be included for practical examination.<br>(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly byexaminers.<br>Students can pick one question (experiment) from the question slot prepared by the internal/external examinersjointly. Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result -60%, Viva-voce 20%of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners) Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be madezero. The duration of SEE is 03hours Rubrics suggested in Annexure-II of Regulation book |

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| | **Suggested Learning Resources:**<br>Textbooks:<br>Dr. P.J.G. Long, Department of Engineering University of Cambridge, "Introduction to Octave," can be downloaded from octavetut.pdf (cam.ac.uk) |

| Data Structures Lab using C | | | |
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| Course Code | 22UEC415C | CIE Marks | 50 |
| Teaching Hours/Week (L:T:P:S) | 0:0:2 | SEE Marks | 50 |
| Total Hours of Pedagogy | 15 Sessions | Total | 100 |
| Credits | 01 | Exam Hours | 03 |

***Additional One hour may be considered for instructionsif required***

**Course objectives:**

- Apply theoretical knowledge of data structures and algorithms to practical programming tasks.
- Gain hands-on experience in implementing and debugging data structures and algorithmsthrough coding exercises and projects.

| Sl. NO. | Experiments |
|---|---|
| 1 | Write a C Program to create a Student record structure to store, N records, each record havingthe structure shown below: USN, Student Name and Semester. Write necessary functions<br>a. To display all the records in the file. b. To search for a specific record based on the USN. In case the record is not found, suitable message should be displayed. Both the options in this case must be demonstrated. (Use pointer to structure for dynamic memory allocation) |
| 2 | Write a C Program to construct a stack of integers and to perform the following operations on it:<br>a. Push b. Pop c. Display The program should print appropriate messages for stack overflow, stack underflow, and stack empty. |
| 3 | Write a C Program to convert and print a given valid parenthesized infix arithmetic expressionto postfix expression. The expression consists of single character operands and the binary operators + (plus), - (minus), * (multiply) and / (divide). |
| 4 | Write a C Program to simulate the working of a queue of integers using an array. Provide thefollowing operations: a. Insert b. Delete c. Display |
| 5 | Write a C Program using dynamic variables and pointers to construct a stack of integers usingsingly linked list and to perform the following operations: a. Push b. Pop c. Display The program should print appropriate messages for stack overflow and stack empty. |
| 6 | Write a C Program to support the following operations on a doubly linked list where each nodeconsists of integers: a. Create a doubly linked list by adding each node at the front. b. Insert a new node to the left of the node whose key value is read as an input c. Delete the node of a given data, if it is found, otherwise display appropriate message. d. Display the contents of the<br>list. (Note: Only either (a, b and d) or (a, c and d) may be asked in the examination) |
| 7 | Write a C Program a. To construct a binary search tree of integers. b. To traverse the tree usingall the methods i.e., in order, preorder and post order. c. To display the elements in the tree. |

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| 8 | Write recursive C Programs for a. Searching an element on a given list of integers using theBinary Search method. b. Solving the Towers of Hanoi problem. |
| 9 | Write a program to traverse a graph using BFS method.<br>Write a program to check whether given graph is connected or not using DFS method. |
| 10 | Design and develop a program in C that uses Hash Function H:K->L as H(K)=K mod m(reminder method) and implement hashing technique to map a given key K to the addressspace L. Resolve the collision (if any) using linear probing |
| Note: The students must be encouraged to create Leet code account and work on Leetcode platform to improve the competency. | |

**Course outcomes (Course Skill Set):**

At the end of the course the student will be able to:

- Develop proficiency in coding and debugging complex algorithms and data structures.
- Acquire practical problem-solving skills by applying data structures and algorithms to real-world programmingchallenges.
- Develop a C program to perform arithmetic operation using data structure and operators.
- Understand the concept of graph theory and develop a C program for searching an element.
- Develop a C program to check the given graph is connected using different algorithms.

**Assessment Details (both CIE and SEE)**

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

**Continuous Internal Evaluation(CIE):**

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record / journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling thelaboratory session and is made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up willbeevaluatedfor10marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-upon time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the $8^{th}$ week of thesemester and these test shall be conducted after the $14^{th}$week of the semester.
- In each test, write-up, conduction of experiment, acceptable result, and procedural knowledge will carry aweightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability. Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40%of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marksscored by the student.

**Semester End Evaluation(SEE):**

SEE marks for the practical course is 50Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University All laboratory experiments are to be included for practical examination.

(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adheredto by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

Students can pick one question (experiment) from the question slot prepared by the internal/external examiners jointly.Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners. General rubrics suggested for SEE are mentioned here, write up-20%, Conduction procedure and result -60%, Viva-voce 20%of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be made zero. Theduration of SEE is 03hours

Rubrics suggested in Annexure-II of Regulation book

**Suggested Learning Resources:**

Textbooks:

- Data Structures using C, Reema Thareja, 2nd Edition, Oxford University Press, 2011
- Introduction to the Design and Analysis of Algorithms, Anany Levitin: 2nd Edition, 2009.Pearson.

- Online Courses:
  - Coursera: "Algorithms" by Princeton University (taught by Robert Sedgewick and Kevin Wayne).
  - edX: "Algorithmic Design and Techniques" (offered by UC San Diego and Higher School of Economics).
- Websites and Online Resources:
  - Geeks for Geeks: Offers a wide range of tutorials, practice problems, and coding challenges related todata structures and algorithms.

    Leet Code: Provides coding challenges that are frequently asked in technical interviews and cover a variety of algorithmic concepts.
  - Hacker Rank: Offers coding challenges and competitions with a focus on algorithms and data structures.
  - Top Coder: Provides algorithmic challenges and competitions for practicing and improving problem-solving skills.
- YouTube Channels:
  - My code school: Offers video tutorials on various data structures and algorithms topics.
  - The Coding Train: Provides interactive coding tutorials on algorithms and data structures.
- Coding Platforms:
  - Code forces: Offers competitive programming challenges to improve algorithmic problem-solving skills. Hackerearth: Provides coding competitions and challenges along with tutorials and practice problems.